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A Bridgeless Buck-Boost Converter-Fed BLDC Motor Drive with Adjustable Speed

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Abstract—

This paper presents a power factor corrected (PFC)bridgeless (BL) buck–boost converter-fed brushless direct current (BLDC) motor drive as a cost-effective solution for low-power applications. An approach of speed control of the BLDC motor by controlling the dc link voltage of the voltage source inverter (VSI) is used with a single voltage sensor. This facilitates the operation of VSI at fundamental frequency switching by using the electronic commutation of the BLDC motor which offers reduced switching losses. A BL configuration of the buck–boost converter is proposed which offers the elimination of the diode bridge rectifier, thus reducing the conduction losses associated with it. A PFC BL buck–boost converter is designed to operate in discontinuous inductor current mode (DICM) to provide an inherent PFC at ac mains. The performance of the proposed drive is evaluated over a wide range of speed control and varying supply voltages (universal ac mains at 90–265 V) with improved power quality at ac mains. The obtained power quality indices are within the acceptable limits of international power quality standards such as the IEC 61000-3-2. The performance of the proposed drive is simulated in MATLAB/Simulink environment, and the obtained results are validated experimentally on a developed prototype of the drive.

Index Terms—Bridgeless (BL) buck–boost converter, brushless direct current (BLDC) motor, discontinuous inductor current mode (DICM), power factor corrected (PFC), power quality.

I. INTRODUCTION

EFFICIENCY and cost are the major concerns in the development of low-power motor drives targeting household applications such as fans, water pumps, blowers, mixers, etc. [1], [2]. The use of the brushless direct current (BLDC) motor in these applications is becoming very common due to features of high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems [1].

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These BLDC motors are not limited to householdapplications, but these are suitable for other applications suchas medical equipment, transportation, HVAC, motion control, and many industrial tools [2]–[4].A BLDC motor has three phase windings on the stator and permanent magnets on the rotor [5], [6]. The BLDC motor is also known as an electronically commutated motor because an electronic commutation based on rotor position is used rather than a mechanical commutation which has disadvantages like sparking and wear and tear of brushes and commutator assembly [5], [6]. Manuscript received January 10, 2013; revised March 25, 2013; accepted June 19, 2013. Date of publication July 24, 2013; date of current version December 20, 2013.Power quality problems have become important issues to be considered due to the recommended limits of harmonics in supply current by various international power quality standards such as the International Electrotechnical Commission (IEC) 61000-3-2 [7]. For class-A equipment (<600 W, 16 A per phase) which includes household equipment, IEC 61000-3-2 restricts the harmonic current of different order such that the total harmonic distortion (THD) of the supply current should be below 19% [7]. A BLDC motor when fed by a diode bridge rectifier (DBR) with a high value of dc link capacitor draws peaky current which can lead to a THD of supply current of the order of 65% and power factor as low as 0.8 [8]. Hence, a DBR followed by a power factor corrected (PFC) converter is utilized for improving the power quality at ac mains. Many topologies of the single-stage PFC converter are reported in the literature which has gained importance because of high efficiency as compared to two-stage PFC converters due to low component count and a single switch for dc link voltage control and PFCoperation [9], [10]. The choice of mode of operation of a PFC converter is a critical issue because it directly affects the cost and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the two modes of operation in which a PFC converter is designed to operate [9], [10]. In CCM, the current in the inductor or the voltage across the intermediate capacitor remains continuous, but it requires the sensing of two voltages
(dc link voltage and supply voltage) and input side current for PFC operation, which is not cost-effective. On the other hand, DCM requires a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch; hence, DCM is preferred for low-power applications [9], [10]. The conventional PFC scheme of the BLDC motor drive utilizes a pulsewidth-modulated voltage source inverter (PWM-VSI) for speed control with a constant dc link voltage.This offers higher switching losses in VSI as the switchinglosses increase as a square function of switching frequency.

As the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed control is achieved by the variable dc link voltage of VSI. This allows the fundamental

frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses.

Singh and Singh [11] have proposed a buck–boost converter feeding a BLDC motor based on the concept of constant dc link voltage and PWM-VSI for speed control which has high switching losses. A single-ended primary-inductance converter (SEPIC)-based BLDC motor drive has been proposed by

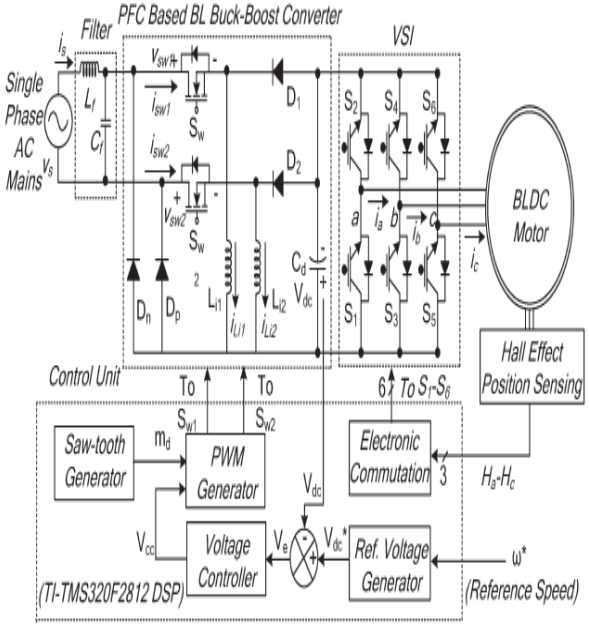


Fig. 1. Proposed BLDC motor drive with front-end BL buck–boost converter

Gopalarathnam and Toliyat [12] but has higher losses in VSIdue to PWM switching and a higher number of current and voltage sensors which restricts its applicability in low-cost application.Singh and Singh [8] have proposed a Cuk converter-fed BLDC motor drive with the concept of variable dc link voltage. This reduces the switching losses in VSI due to the fundamental switching frequency operation for the electronic commutation of the BLDC motor and to the variation of the speed by controlling the voltage at the dc bus of VSI. A CCM operation of the Cuk converter has been utilized which requires three sensors and is not encouraged for low cost and low power rating. For further improvement in efficiency, bridgeless (BL) converters are used which allow the elimination of DBR in the front end [13]–[21]. A buck–boost converter configuration is best suited among various BL converter topologies for applications requiring a wide range of dc link voltage control (i.e., bucking and boosting mode). Jang and Jovanovi´c [13] and Huber *et al.*[14] have presented BL buck and boost converters, respectively. These can provide the voltage buck [13] or voltage boost [14], [15] which limits the operating range of dc link voltage control. Wei *et al.* [16] have proposed a BL buck–boost converter but use three switches which is not a cost-effective solution. A new family of BL SEPIC and Cuk converters has been reported in the literature [17]–[21] but requires a large number of components and

has losses associated with it. This paper presents a BL buck–boost converter-fed BLDC motor drive with variable dc link voltage of VSI for improved
power quality at ac mains with reduced components.

II. PROPOSED PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed BL buck–boost converter-based VSI-fed BLDC motor drive. The parameters of the BL buck–boost converter are designed such that it operates in discontinuous inductor current mode (DICM) to achieve an inherent power factor correction at ac mains. The speed control of BLDC motor is achieved by the dc link voltage controlof VSI using a BL buck–boost converter. This reduces the switching losses in VSI due to the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated for a wide range of speed control with improved power quality at ac mains. Moreover, the effect of supply voltage variation at universal ac mains is also studied to demonstrate the performance of the drive in practical supply conditions. Voltage and current stresses on the PFC converter switch are also evaluated for determining the switch rating and heat sink design. Finally, a hardware implementation of the proposed BLDC motor drive is carried out to demonstrate the feasibility of the proposed drive over a wide range of speed control with improved power quality at ac mains.

TABLE I
COMPARATIVE ANALYSIS OF PROPOSED BL BUCK–BOOST CONVERTER WITH EXISTING TOPOLOGIES

Configuration	No. of Devices					½ Period Cond.	Suit-ability
	S_w	D	L	C	Total		
BL-Buck [13]	2	4	2	2	10	5	No
BL-Boost [14]	2	2	1	1	6	4	No
BL-Boost [15]	2	2	1	2	7	7	No
BL-Buck-Boost [16]	3	4	1	3	11	8	Yes
BL-Cuk T-1 [17, 18]	2	3	3	3	11	7	Yes
BL-Cuk T-2 [17, 18]	2	2	3	4	11	11	Yes
BL-Cuk T-3 [17, 18]	2	4	4	3	13	7	Yes
BL-Cuk [19]	2	3	3	2	10	8	Yes
BL-SEPIC [20]	2	3	1*	3	9	7	Yes
BL-SEPIC [21]	2	3	2	2	9	7	Yes
Proposed	2	4	2	1	9	5	Yes

*- Coupled Inductor

A brief comparison of various configurations reported in the literature is tabulated in Table I. The comparison is carried out on the basis of the total number of components (switch—*S*w, diode—D, inductor—L, and capacitor—C) and total numberof components conducting during each half cycle of supply voltage. The BL buck [13] and boost [14], [15] converter

configurations are not suitable for the required application due to the requirement of high voltage conversion ratio.

The proposed configuration of the BL buck–boost converter has the minimum number of components and least number ofconduction devices during each half cycle of supply voltagewhich governs the choice of the BL buck–boost converter for this application.

III. OPERATING PRINCIPLE OF PFC BL BUCK–BOOST CONVERTER

The operation of the PFC BL buck–boost converter is classified into two parts which include the operation during the positive and negative half cycles of supply voltage and during the complete switching cycle.

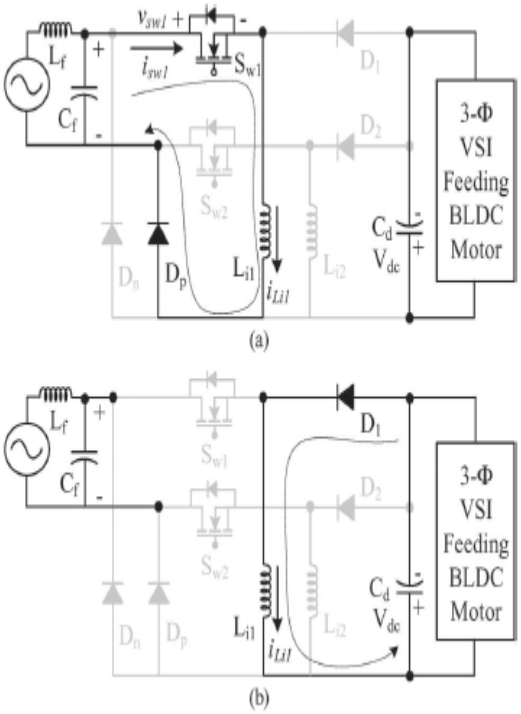
A. Operation During Positive and Negative Half Cycles of Supply Voltage

In the proposed scheme of the BL buck–boost converter, switches *Sw*1 and *Sw*2 operate for the positive and negative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch *Sw*1, inductor *Li*1, and diodes *D*1 and *Dp*are operated to transfer energy to dc link capacitor *Cd* as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch *Sw*2, inductor *Li*2, and diodes *D*2 and *Dn*conduct as shown in Fig. 3(a)–(c). In the DICM operation of the BL buck–boost converter, the current in inductor *Li* becomes discontinuous for a certainduration in a switching period. Fig. 2(d) shows the waveforms of different parameters during the positive and negative half cycles of supply voltage.

B. Operation During Complete Switching Cycle

Three modes of operation during a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter. *Mode I:* In this mode, switch *Sw*1 conducts to charge the inductor *Li*1; hence, an inductor current *i*Li1 increases in this mode as shown in Fig. 2(a). Diode *Dp*completes the input side circuitry, whereas the dc link capacitor *Cd* is discharged by the VSI-fed BLDC motor as shown in Fig. 3(d). *Mode II:* As shown in Fig. 2(b), in this mode of operation, switch *Sw*1 is turned off, and the stored energy in inductor *Li*1 is transferred to dc link capacitor *Cd* until the inductor iscompletely discharged. The current in inductor *Li*1 reduces and reaches zero as shown in Fig. 3(d).*Mode III:* In this mode, inductor *Li*1 enters discontinuous

conduction, i.e., no energy is left in the inductor; hence, current *i*Li1 becomes zero for the rest of the switching period. As shown in Fig. 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor *Cd* supplies energy to the load;hence, voltage *V*dc across dc link capacitor *Cd* starts decreasing.The operation is repeated when switch *Sw*1 is turned on again after a complete switching cycle.



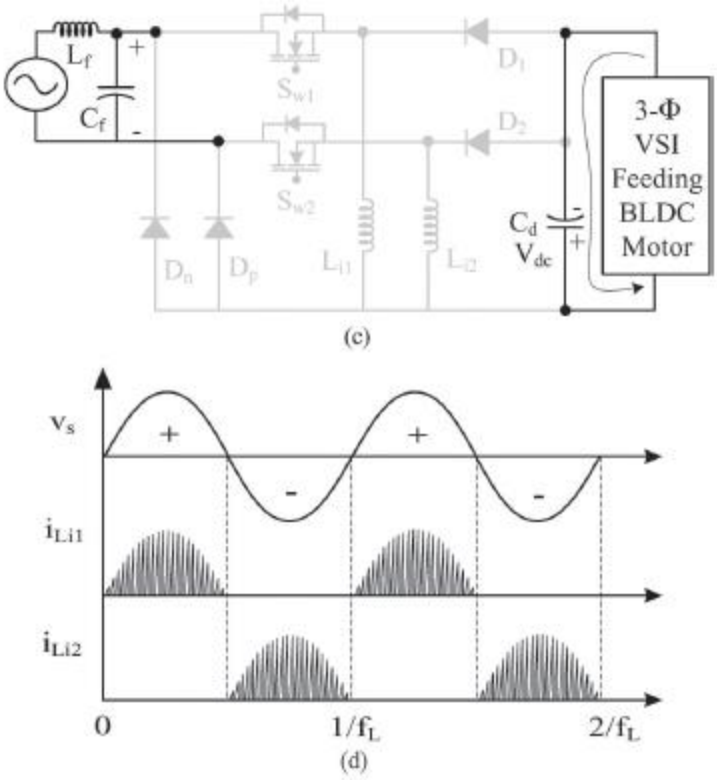


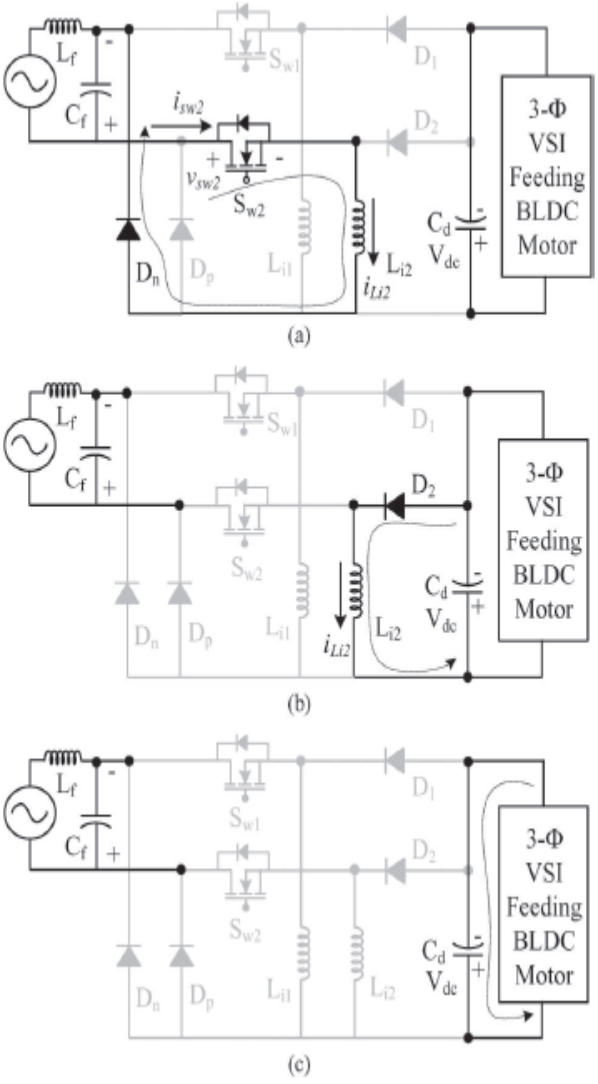
Fig. 2.Operation of the proposed converter in different modes (a)–(c) fora positive half cycle of supply voltage and (d) the associated waveforms.

(a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms for positive and negative half cycles of supply voltage.Similarly, for the negative half cycle of the supply voltage, switch *Sw*2, inductor *Li*2, and diodes *Dn*and *D*2 operate for voltage control and PFC operation.

IV. DESIGN OF PFC BL BUCK–BOOST CONVERTER

A PFC BL buck–boost converter is designed to operate in DICM such that the current in

inductors *Li*1 and *Li*2 becomes discontinuous in a switching period. For a BLDC of power rating 251 W (complete specifications of the BLDC motor are given in the Appendix), a power converter of 350 W (*Po*) is



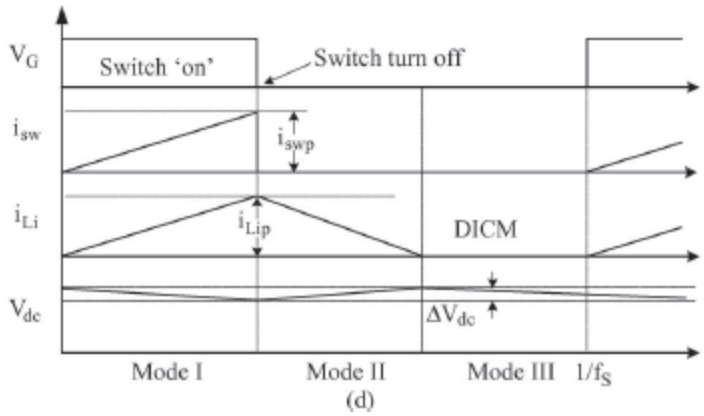


Fig. 3. Operation of the proposed converter in different modes (a)–(c) for
a negative half cycle of supply voltage and (d) the associated waveforms.
(a)Mode I. (b)Mode II. (c)Mode III. (d)Waveforms during complete switching
cycle.

designed. For a supply voltage with an rms value of 220 V, the
average voltage appearing at the input side is given as [24]

$$V_{\text{in}} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} \approx 198 \text{ V}. \qquad (1)$$

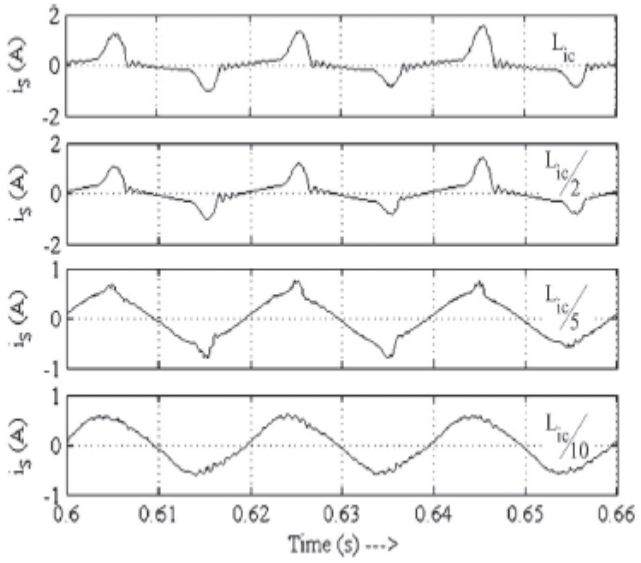


Fig. 4. Supply current at the rated load on BLDC motor for different valuesof input side inductors with supply voltage as 220 V and dc link voltage as 50 V.

The proposed converter is designed for dc link voltage control from 50 V (*V*dc min) to 200 V (*V*dcmax) with a nominal value (*V*dc des) of 100 V; hence, the minimum and the maximum duty ratio (*d*min and *d*max) corresponding to *V*dc min and *V*dcmax are calculated as 0.2016 and 0.5025, respectively.

A. Design of Input Inductors (Li1 and Li2)

The value of inductance *L*ic1, to operate in critical conduction mode in the buck–boost converter, is given as [23]

$$L_{\text{ic1}} = \frac{R(1-d)^2}{2f_s} \tag{3}$$

where*R* is the equivalent load resistance, *d* is the duty ratio,and*f*sis the switching frequency. Now, the value of *L*ic1 is calculated at the worst duty ratio of *d*min such that the converter operates in DICM even at very low duty ratio. At minimum duty ratio, i.e., the BLDC motor operating at 50 V (*V*dc min), the power (*P*min) is given as 90 W (i.e., for constant torque, the load power is proportional to speed). Hence, from (4), the value of inductance *L*ic min corresponding to *V*dc min is calculated as

$$L_{\text{ic min}} = \frac{V_{\text{dc min}}^2}{P_{\text{min}}}\frac{(1-d_{\text{min}})^2}{2f_s} = \frac{50^2}{90}\frac{(1-0.2016)^2}{2\times 20000} = 442.67\,\mu\text{H}. \tag{4}$$

The values of inductances *Li*1 and *Li*2 are taken less than 1/10th of the minimum critical value of inductance to ensure a deep DICM condition [24]. The analysis of supply current at minimum duty ratio (i.e., supply voltage as 220 V and dc link voltage as 50 V) is carried out for different values of the inductor (*Li*1 and *Li*2). Fig. 4 shows the supply current at the input inductor's value as *L*ic, *L*ic/2, *L*ic/5, and *L*ic/10, respectively. The supply current at higher values of the inputside inductor is highly distorted due to the inability of the converter to operate in DICM at peak values of supply voltages. Hence, the values of inductors *Li*1 and *Li*2 are selected around 1/10th of the critical inductance and are taken as 35 μH. It reduces the size, cost, and weight of the PFC converter.

B. Design of DC Link Capacitor (Cd)

The design of the dc link capacitor is governed by the amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows. For the PFC operation, the supply current (*is*) is in phase with the supply voltage (*vs*). Hence, the input power *P*in is

given as [22]

$$P_{\text{in}} = \sqrt{2}V_S\text{Sin}\omega t * \sqrt{2}I_S\text{Sin}\omega t = V_S I_S(1-\text{Cos}2\omega t) \tag{5}$$

where the latter term corresponds to the second-order harmonic,which is reflected in the dc link capacitor as

$$i_C(t) = -\frac{V_S I_S}{V_{\rm dc}} \text{Cos} 2\omega t. \quad (6)$$

The dc link voltage ripple corresponding to this capacitor current is given as [22]

$$\Delta V_{\rm dc} = \frac{1}{C_d}\int i_C(t)dt = -\frac{I_d}{2\omega C_d}\text{Sin} 2\omega t. \quad (7)$$

For a maximum value of voltage ripple at the dc link capacitor, Sin(ωt) is taken as 1. Hence, (7) is rewritten as

$$C_d = \frac{I_d}{2\omega \Delta V_{\rm dc}}. \quad (8)$$

Now, the value of the dc link capacitor is calculated for the designed value *V*dc des with permitted ripple in the dc link voltage (ΔVdc) taken as 3% as

$$C_d = \frac{I_d}{2\omega \Delta V_{\rm dc}} = \frac{P_o/V_{\rm dc\,des}}{2\omega \Delta V_{\rm dc}} = \frac{350/100}{2\times 314\times 0.03\times 100} = 1857.7\ \mu\text{F}. \quad (9)$$

Hence, the nearest possible value of dc link capacitor *Cd* is selected as 2200 μF.

C. Design of Input Filter (Lf and Cf)

A second-order low-pass *LC* filter is used at the input side to absorb the higher order harmonics such that it is not reflected in the supply current. The maximum value of filter capacitanceis given as [25]

$$C_{\max} = \frac{I_{\rm peak}}{\omega_L V_{\rm peak}} \tan(\theta) = \frac{350}{220}\frac{1}{314\ \times 220\sqrt{2}} \text{t} = 401.98\ \text{nF}$$

where*I*peak, *V*peak, ωL, and θ represent the peak value of supply current, peak value of supply voltage, line frequency in radians per second, and displacement angle between the supply voltage and supply current, respectively. Hence, a value of *Cf*is taken as 330 nF. Now, the value of inductor *Lf* is calculated as follows. The value of the filter inductor is designed by consideringthe source impedance (*Ls*) of 4%–5% of the base impedance. Hence, the additional value of inductance required is given as

$$L_f = L_{\rm req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{\rm req} + 0.04\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{P_o}\right)$$
$$L_{\rm req} = \frac{1}{4\pi^2 \times 2000^2 \times 330 \times 10^{-9}} - 0.04\left(\frac{1}{314}\right)\left(\frac{220^2}{350}\right) = 1.57\ \text{mH} \quad (11)$$

where*fc* is the cutoff frequency of the designed filter which is selected as [25]

$$f_L < f_c < f_{\rm sw}. \quad (12)$$

Hence, a value of *fc* is taken as *f*sw/10. Finally, a low-pass filter with inductor and capacitor of
1.6 mH and 330 nF is selected for this particular application.

V. CONTROL OF PFC BL BUCK–BOOST CONVERTER-FEDBLDC MOTOR DRIVE

The control of the PFC BL buck–boost converter-fed BLDC motor drive is classified into two parts as follows.

A. Control of Front-End PFC Converter: Voltage Follower Approach

The control of the front-end PFC converter generates the PWM pulses for the PFC converter switches (*Sw*1 and *Sw*2) for dc link voltage control with PFC operation at ac mains. A single voltage control loop (voltage follower approach) is utilized for

the PFC BL buck–boost converter operating in DICM. A reference dc link voltage (*V*∗dc) is generated as

$$V_{\rm dc}^{*} = k_v \omega^{*} \qquad (13)$$

where*kv*and $\omega*$are the motor's voltage constant and the reference speed, respectively. The voltage error signal (*Ve*) is generated by comparing the reference dc link voltage (*V* ∗dc) with the sensed dc link voltage (*V*dc) as

$$V_e(k) = V_{\rm dc}^{*}(k) - V_{\rm dc}(k) \qquad (14)$$

where*k* represents the *k*th sampling instant.This error voltage signal (*Ve*) is given to the voltage proportional–integral (PI) controller to generate a controlled output voltage (*V*cc) as

$$V_{cc}(k) = V_{cc}(k-1) + k_p \{V_e(k) - V_e(k-1)\} +$$

where*kp*and *ki*are the proportional and integral gains of the voltage PI controller. Finally, the output of the voltage controller is compared with a high frequency sawtooth signal (*md*) to generate the PWM pulses as

$$\text{For } v_s > 0; \quad \begin{cases} \text{if } m_d < V_{cc} \text{ then } S_{w1} = \text{'ON'} \\ \text{if } m_d \geq V_{cc} \text{ then } S_{w1} = \text{'OFF'} \end{cases}$$

$$\text{For } v_s < 0; \quad \begin{cases} \text{if } m_d < V_{cc} \text{ then } S_{w2} = \text{'ON'} \\ \text{if } m_d \geq V_{cc} \text{ then } S_{w2} = \text{'OFF'} \end{cases}$$

where*Sw*1 and *Sw*2 represent the switching signals to the switches of the PFC converter.

B. Control of BLDC Motor: Electronic Commutation

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical

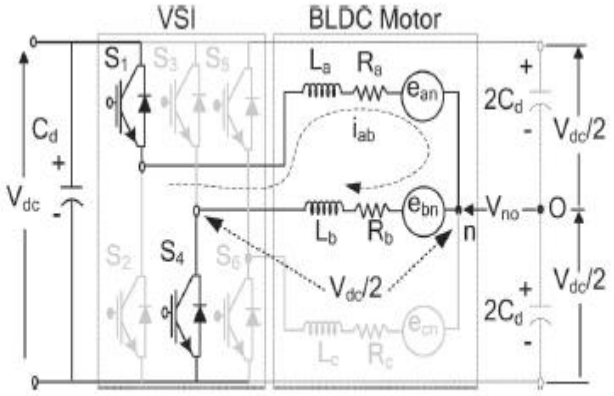


Fig. 5. Operation of a VSI-fed BLDC motor when switches S_1 and S_4 are conducting.

TABLE II
SWITCHING STATES FOR ACHIEVING ELECTRONIC COMMUTATION OF BLDC MOTOR BASED ON HALL-EFFECT POSITION SIGNALS

θ (°)	Hall Signals			Switching States					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

dc current is drawn from the dc link capacitor for 120◦and placed symmetrically at the center of each phase. A Hall-effect position sensor is used to sense the rotor position on a span of 60◦, which is required for the electronic commutation of the BLDC motor. The conduction states of two switches (*S*1 and *S*4) are shown in Fig. 5. A line current *i*abis drawn from the dc link capacitor whose magnitude depends on the

applied dc link voltage (*V*dc), back electromotive forces (EMFs) (*e*anand *e*bn), resistances (*Ra* and *Rb*), and self-inductance and mutual inductance (*La*, *Lb*, and M) of the stator windings. Table II shows the different switching states of the VSI feeding a BLDC motor based on the Hall-effect position signals (*Ha* −*Hc*). A
brief modeling of the BLDC motor is given in the Appendix.

VI. SIMULATED PERFORMANCE OF PROPOSED BLDC MOTOR DRIVE

The performance of the proposed BLDC motor drive is simulated in MATLAB/Simulink environment using the Sim-Power-System toolbox. The performance evaluation of the proposed
drive is categorized in terms of the performance of the BLDC motor and BL buck–boost converter and the achieved power quality indices obtained at ac mains. The parameters associated with the BLDC motor such as speed (N), electromagnetic torque (*Te*), and stator current (*ia*) are analyzed for the proper functioning of the BLDC motor. Parameters such assupply voltage (*Vs*), supply current (*is*), dc link voltage (*V*dc), inductor's currents (*i*Li1, *i*Li2), switch voltages (*V*sw1, *V*sw2), and switch currents (*i*sw1, *i*sw2) of the PFC BL buck–boost
converter are evaluated to demonstrate its proper functioning.

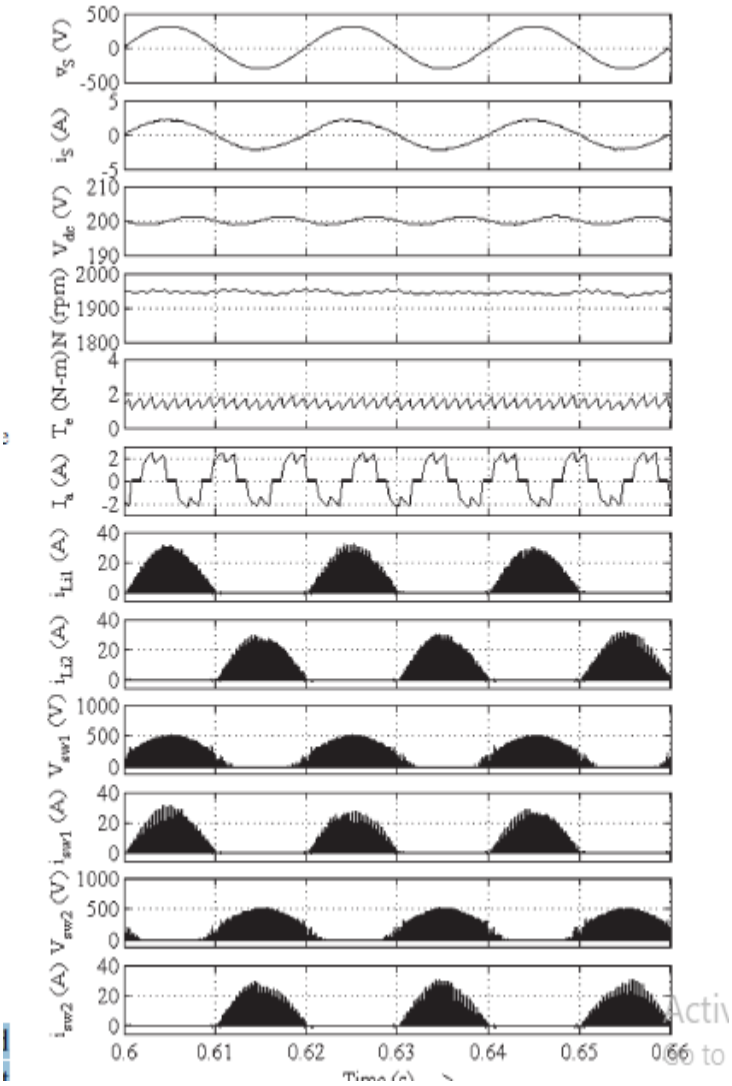


Fig. 6. Steady-state performance of the proposed BLDC motor drive at rated conditions.

Moreover, power quality indices such as power factor (PF),displacement power factor (DPF), crest factor (CF), and THD of supply

current are analyzed for determining power quality at
ac mains.

A. Steady-State Performance

The steady-state behavior of the proposed BLDC motor drive for two cycles of supply voltage at rated condition (rated dc link voltage of 200 V) is shown in Fig. 6. The discontinuous inductor
currents (*i*Li1 and *i*Li2) are obtained, confirming the DICM operation of the BL buck–boost converter. The performance of the proposed BLDC motor drive at speed control by varying dc link voltage from 50 to 200 V is tabulated in Table III. The harmonic spectra of the supply current at rated and light load conditions, i.e., dc link voltages of 200 and 50 V, are also shown
in Fig. 7(a) and (b), respectively, which shows that the THD of supply current obtained is under the acceptable limits of IEC 61000-3-2.

B. Dynamic Performance of Proposed BLDC Motor Drive

The dynamic behavior of the proposed drive system during a starting at 50 V, step change in dc link voltage from 100 to 150 V, and supply voltage change from 270 to 170 V is shown

TABLE III
PERFORMANCE OF PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE UNDER SPEED CONTROL

V_{dc} (V)	N (rpm)	DPF	THD of I_s (%)	PF	I_s (A)
50	380	0.9845	7.1	0.982	0.3714
60	460	0.9866	6.37	0.9846	0.4401
70	570	0.9907	5.87	0.989	0.5106
80	680	0.9928	5.38	0.9914	0.5811
90	790	0.9942	5.09	0.9929	0.6543
100	900	0.9951	4.91	0.9939	0.7274
110	1000	0.9959	4.75	0.9948	0.8023
120	1110	0.9972	4.56	0.9962	0.8771
130	1220	0.9977	4.49	0.9967	0.955
140	1330	0.9979	4.37	0.9969	1.033
150	1430	0.9984	4.21	0.9975	1.11
160	1530	0.9988	3.96	0.998	1.187
170	1660	0.999	3.91	0.9982	1.272
180	1800	0.9993	3.89	0.9985	1.356
190	1880	0.9993	3.87	0.9986	1.437
200	1960	0.9996	3.85	0.9989	1.517

Fig. 7. Harmonic spectra of supply current at rated supply voltage and rated

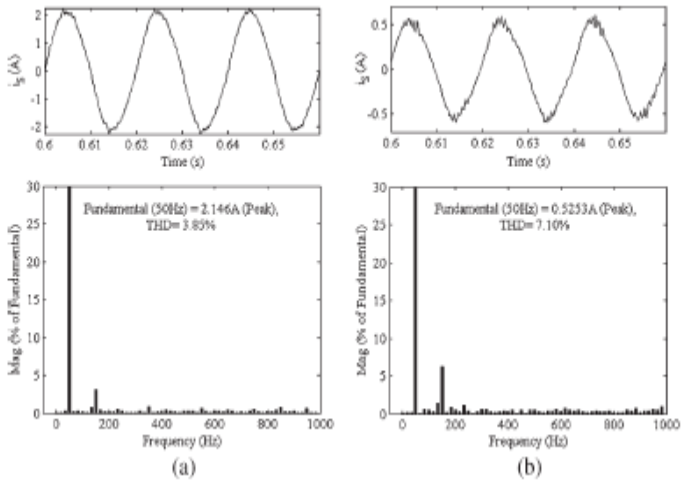


Fig. 7. Harmonic spectra of supply current at rated supply voltage and ratedloading on BLDC motor for a dc link voltage of (a) 200 V and (b) 50 V.

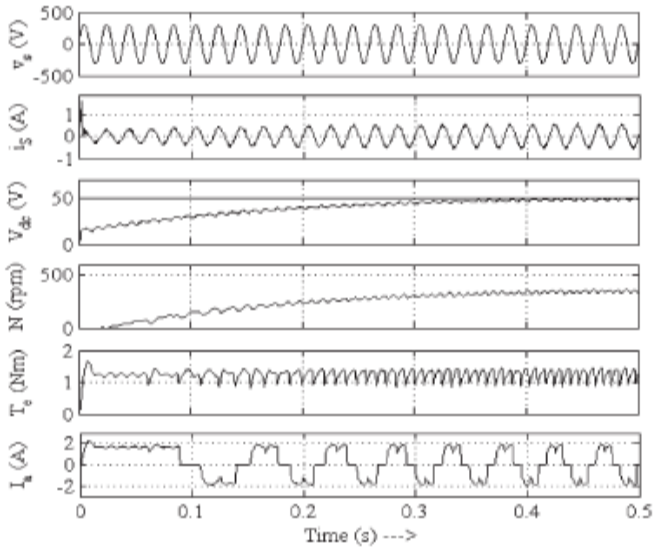
in Fig. 8. A smooth transition of speed and dc link voltage is achieved with a small

overshoot in supply current under the acceptable limit of the maximum allowable stator windingcurrent of the BLDC motor. The controller gains are given in the Appendix.

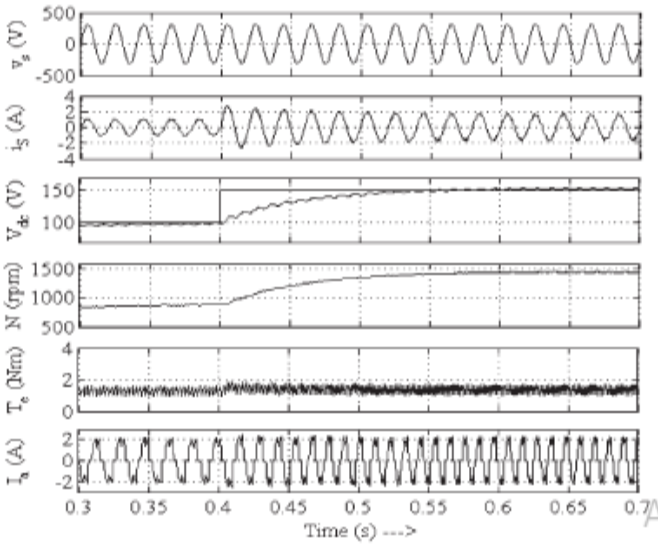
C. Performance Under Supply Voltage Variation

The behavior of the proposed BLDC motor drive in practical supply conditions is demonstrated, and the performance is also evaluated for supply voltage from 90 to 270 V. Table IV shows different power quality indices with variation in supply voltage. The THD of supply current obtained is within the limits of IEC 61000-3-2. Fig. 9(a) and (b) shows the harmonic spectra

of supply current at ac mains at rated conditions of dc link voltage and load on the BLDC motor with supply voltage as 90 and 270 V, respectively. An acceptable THD of supply current is obtained for both the cases which show an improved power quality operation of the proposed BLDC motor drive at universal ac mains.



(a)



(b)

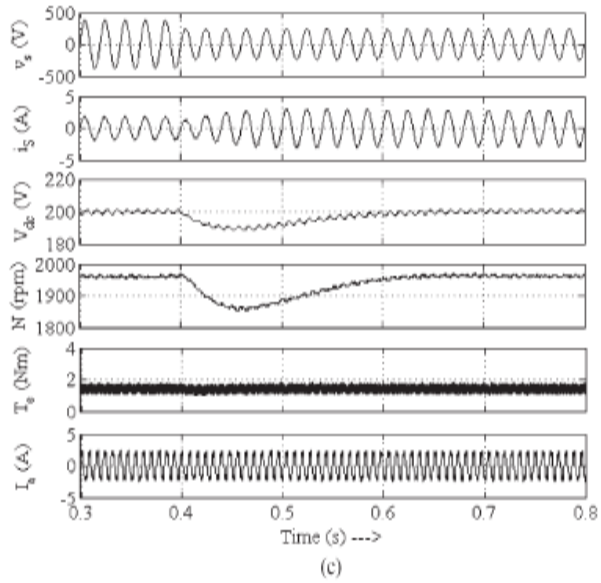


Fig. 8. Dynamic performance of proposed BLDC motor drive during
(a) starting, (b) speed control, and (c) supply voltage variation at rated
conditions.

D. Stress on PFC Converter Switches

Voltage and current stresses on PFC switches for different
loading on the BLDC motor are tabulated in Table V. The
switch's peak voltage (V_{sw}) and peak current (i_{peak}) and the
rms current (i_{rms}) flowing through the switch are tabulated

TABLE IV
PERFORMANCE OF PFC BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE UNDER VARYING SUPPLY VOLTAGE

V_s (V)	DPF	THD of I_s(%)	PF	I_s (A)	CF
90	0.9923	1.46	0.9922	3.915	1.414
110	0.9943	1.84	0.9941	3.256	1.414
130	0.9959	2.3	0.9956	2.596	1.414
150	0.9984	2.6	0.9981	2.281	1.414
170	0.9997	2.9	0.9993	1.968	1.414
190	0.9998	3.2	0.9993	1.781	1.414
210	0.9998	3.37	0.9992	1.591	1.414
230	0.9993	3.94	0.9985	1.463	1.414
250	0.9987	4.63	0.9976	1.335	1.414
270	0.9981	4.74	0.997	1.236	1.414

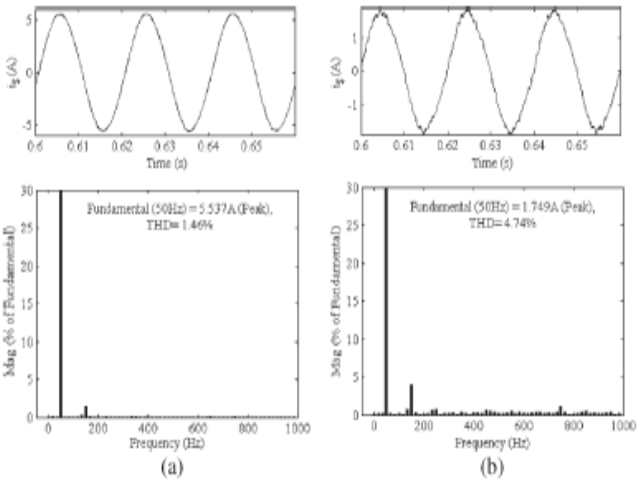


Fig. 9. Harmonic spectra of supply current at rated loading on BLDC motor with dc link voltage as 200 V and supply voltage as (a) 90 V and (b) 270 V.

TABLE V
VOLTAGE AND CURRENT STRESSES UNDER DIFFERENT LOADING

Load (%)	V_{SW} (V)	I_{swp} (A)	I_{swr} (A)
10	510	16	0.2084
20	510	17	0.2757
30	510	19	0.3429
40	510	22	0.4101
50	510	23	0.4791
60	510	24	0.548
70	510	24	0.5923
80	510	25	0.6364
90	510	26	0.6983
100	510	27	0.7602

for load variation on the BLDC motor from 10% to 100%of the rated load. The switch's peak voltage and peak currentare required for selecting the PFC switch rating while therms current flowing through the switch decides the size of the required heat sink. The simulated performance of the proposed drive is found to be satisfactory in all aspects.

VII. HARDWARE VALIDATION OF PROPOSED BLDC MOTOR DRIVE

A digital signal processor (DSP) based on TI-TMS320F2812 is used for the development of the proposed PFC BL buck–boost converter-fed BLDC motor drive. The necessary circuitry for isolation between DSP and gate drivers of solid-

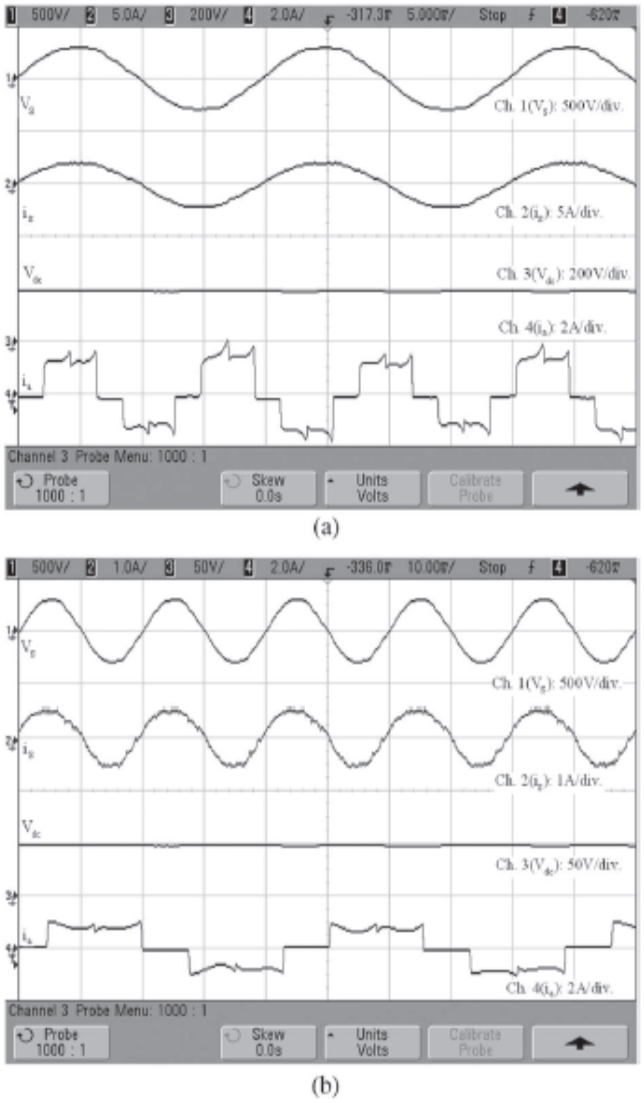


Fig. 10. Steady-state performance of the proposed BLDC motor drive at ratedconditions with dc link voltage as (a) 200 V and (b) 50 V.state switches is developed using the optocoupler 6N136. Aprefiltering and isolation circuit for the Hall-Effect sensor isalso developed for sensing the Hall-effect position signals. Test results are discussed in the following sections.

A. Steady-State Performance

Fig. 10(a) and (b) shows the operation of the proposed BLDC motor drive showing supply voltage (*vs*), supply current (*is*), dc link voltage (*V*dc), and stator current (*ia*) for the dc link voltages of 200 and 50 V, respectively. A sinusoidal supply current in phase with the supply voltage is achieved for operation at both dc link voltages which shows a near unity power factor at ac mains. The variation of speed and the dc link voltage with input reference voltage at the analog-to-digitalconverter of DSP is tabulated in Table VI.

B. Operation of PFC BL Buck–Boost Converter

Fig. 11(a) and (b) shows the currents flowing in inductors *Li*1 and *Li*2 and its enlarged waveforms, each appearing for the positive and negative half cycles of the supply voltage for the necessary operation of the BL buck–boost converter. It clearly demonstrates the DICM operation of the BL buck–boost converter.

TABLE VI
VARIATION OF DC LINK VOLTAGE AND SPEED WITH REFERENCE VOLTAGE

V_{ref} (V)	0.5	0.75	1	1.25	1.5	1.75	2	2.25	2.5
V_{dc} (V)	40	60	80	100	120	140	160	180	200
Speed (rpm)	370	600	790	990	1180	1370	1560	1780	1970

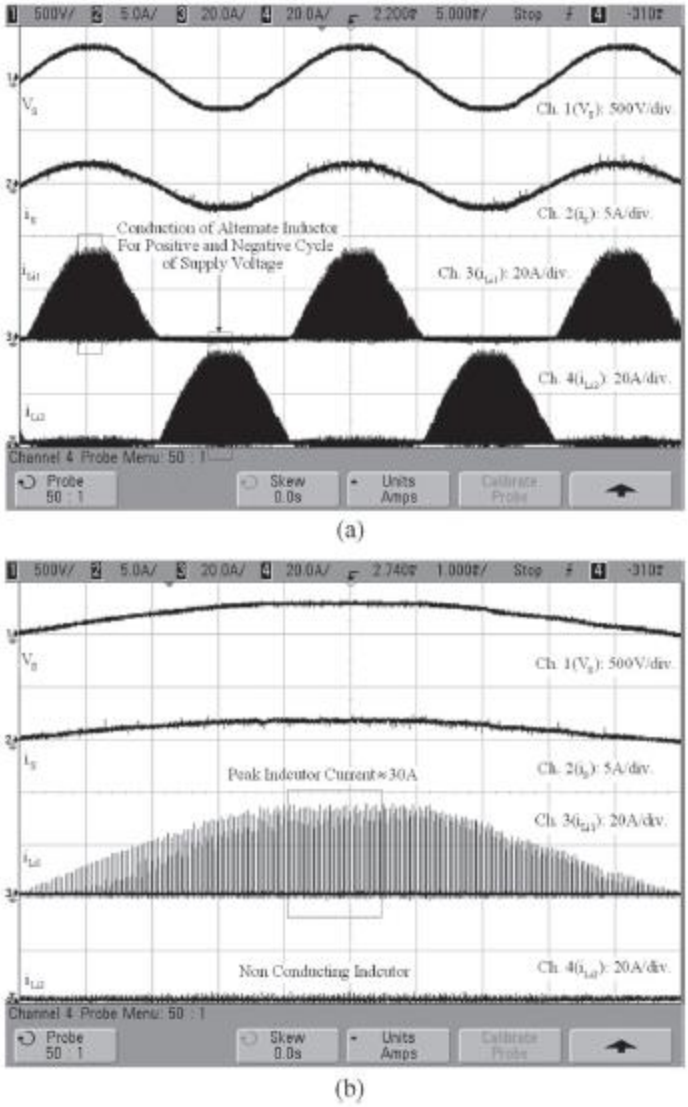


Fig. 11.(a) Variation of inductor's currents (*iLi*1 and *iLi*2) and (b) itsenlarged waveforms with supply voltage and supply current.

C. Stress on PFC Converter Switches

Fig. 12(a) and (b) shows the switch currents (*i*sw1, *i*sw2) and voltages (*V*sw1, *V*sw2) appearing for each half cycle and its enlarged waveforms, respectively. A peak voltage of 500 V and a current stress of 28 A

are achieved, which is quite acceptable and in accordance with the simulated results.

D. Dynamic Performance of Proposed BLDC Motor Drive

The dynamic performance of the proposed BLDC motor drive during starting, speed control, and supply voltage variationis shown in Fig. 13. As shown in Fig. 13(a), a limited inrushcurrent is obtained during the starting of the BLDC motor at 50 V. Moreover, a limited transient in supply current is obtained

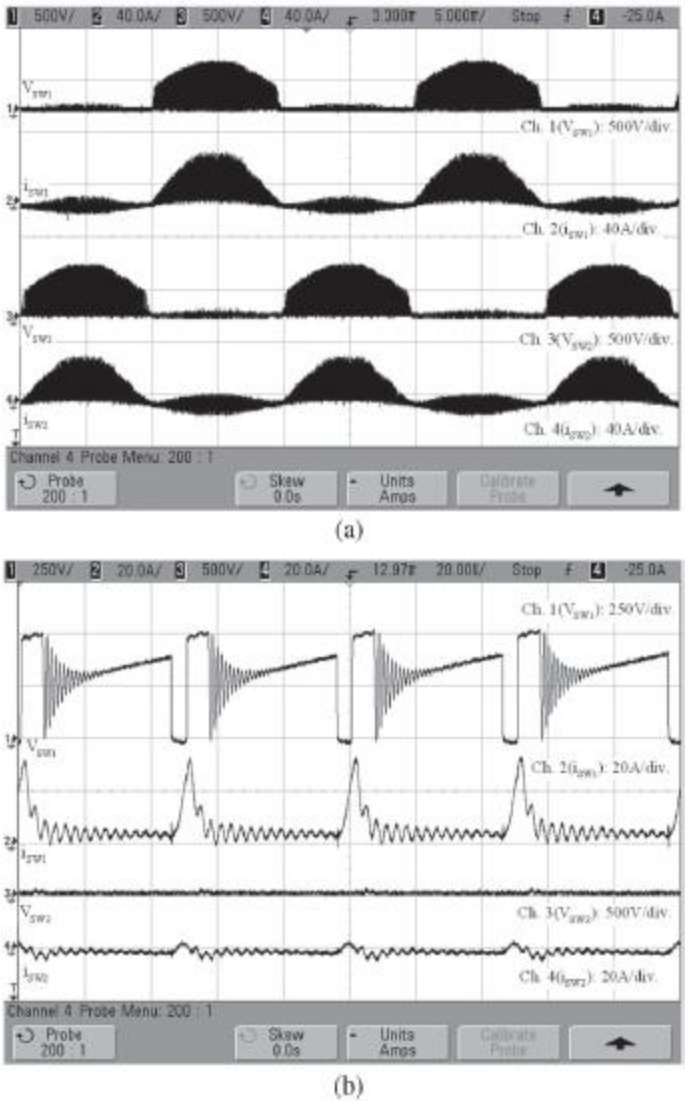


Fig. 12. (a) Stress on PFC converter switches and (b) its enlarged waveformsduring the operation of proposed BLDC motor drive at rated conditions.for change in dc link voltage and supply voltage as shown in Fig. 13(b) and (c), respectively. The controller gains are given in the Appendix.

E. PFC and Improved Power Quality Operation

The performance parameters and the power quality indices such as supply voltage (*vs*), supply current (*is*), active (*P*ac), reactive (*Pr*), and apparent (*Pa*) powers, PF, DPF, and THD ofsupply current are measured on a "Fluke" make power quality analyzer. Fig. 14(a)–(c) and (d)–(f) shows the obtained indicesat rated condition of the BLDC motor with dc link voltages as

200 and 50 V, respectively. Moreover, Fig. 14(g)–(i) and (j)–(l) shows the performance at supply voltages of 90 and 270 V, respectively. An improved power quality is obtained in all these conditions with power quality indices within the limits of IEC 61000-3-2 [7].

VIII. COMPARATIVE ANALYSIS OF DIFFERENT CONFIGURATIONS

A comparative analysis of the proposed BL buck–boost converter-fed BLDC motor drive is carried out with conventional schemes. Two conventional schemes of the DBR-fed

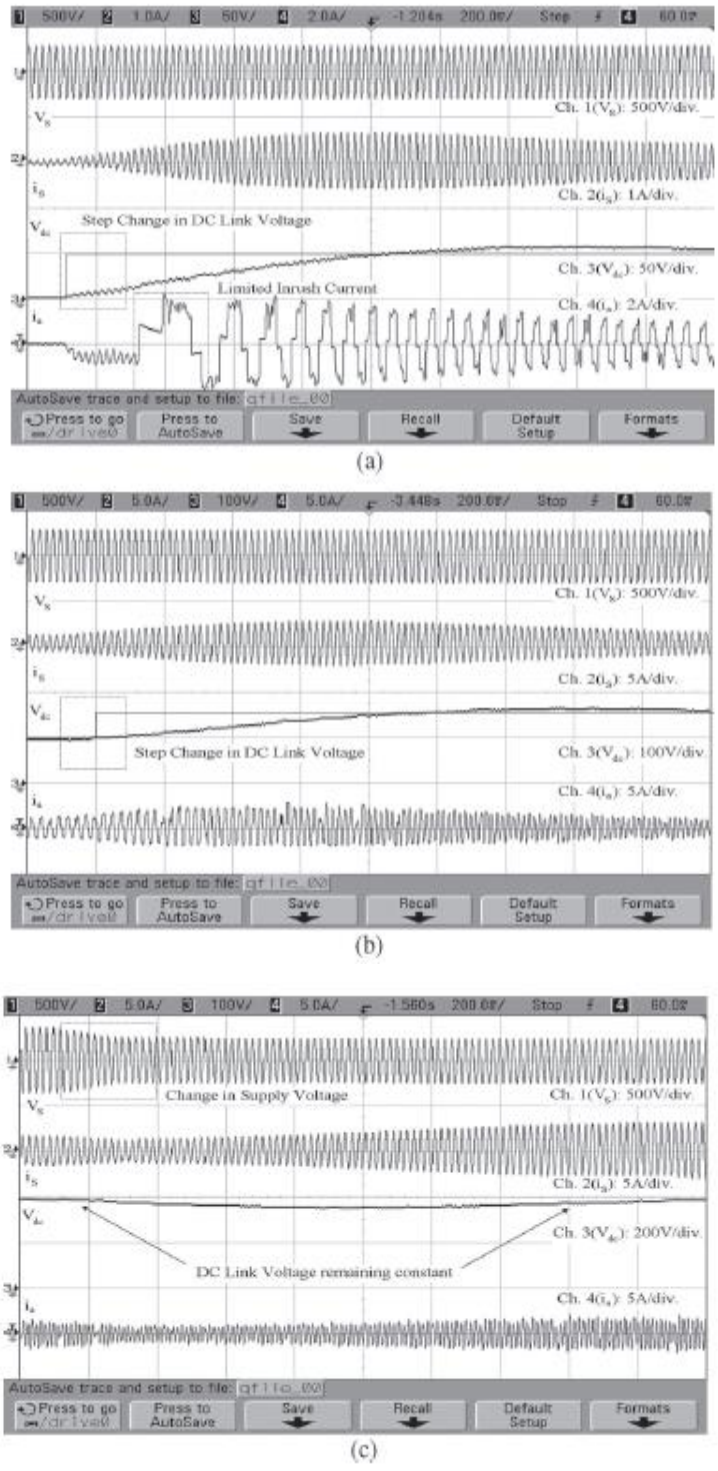


Fig. 13. Dynamic behavior of the proposed BLDC motor drive during(a) starting at dc link voltage of 50 V, (b) step change in dc link voltage from 100 to 150 V, and (c)

supply voltage variation. BLDC motor drive and a single-switch PFC using a constant dc bus voltage are used for comparative performance evaluation. The analysis is classified into two subcategories as follows.

A. Comparison on Basis of Losses and Efficiency

The losses in the complete BLDC motor drive are classified as losses in various sections such as DBR, PFC converter, VSI,and the BLDC motor. The losses in different parts of the BLDC motor are measured for three different configurations of the BLDC motor drive. As shown in Fig.15(a), the losses in two conventional schemes of the BLDC motor drive are higher in VSI due to the use of PWM-based switching of VSI which increases the switching losses in the system. This accounts for

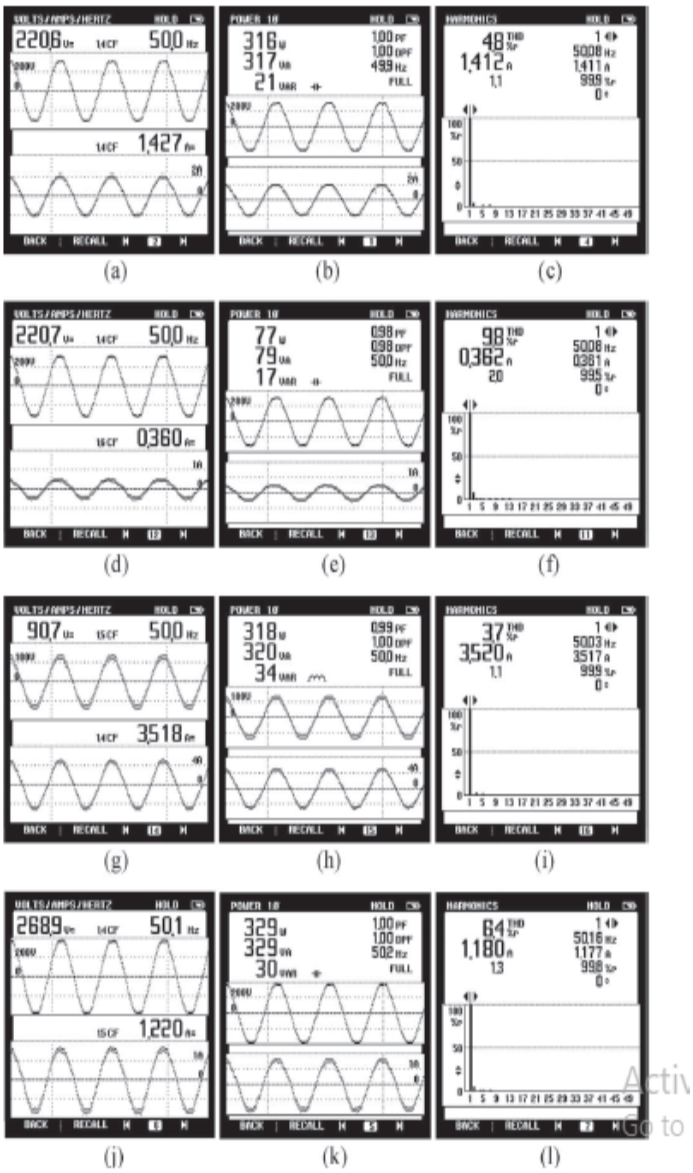


Fig. 14. Power quality indices and performance parameters (*vs*, *is*, *P*ac, *Pa*,*Pr*, PF, DPF, CF, and harmonic spectrum of *is*) of proposed BLDC motor drive at rated load on BLDC motor with (a)–(c) dc link voltage as 200 V and supply voltage as 220 V, (d)–(f) dc link voltage as 50 V and supply voltage as 220 V,(g)–(i) dc link voltage as 200 V and supply voltage as 90 V, and (j)–

(l) dc link voltage as 200 V and supply voltage as 270 V. an increase in the efficiency of the proposed system as shown in Fig. 15(b). The conventional scheme of the BLDC motor drivewith PFC has the lowest efficiency due to the high amount of losses in the VSI as well as in the DBR and PFC converter.

B. Comparison on Basis of Power Quality

Fig. 16(a) shows the THD of supply current at ac mains with output power for both the conventional and the proposed scheme of the BL buck–boost converter-fed BLDC motor drive.

The harmonic distortion in a conventional scheme of the DBRfedBLDC motor drive is as high as 80%–100%, which is not a recommended solution as per the guidelines of IEC 61000- 3-2 [7]. Fig. 16(b) shows the power factor with output power for these three different configurations. The harmonic distortion and power factor in a conventional scheme using a singleswitchPFC are also under the acceptable limits but have higher losses associated with it as shown in Fig. 15(a).

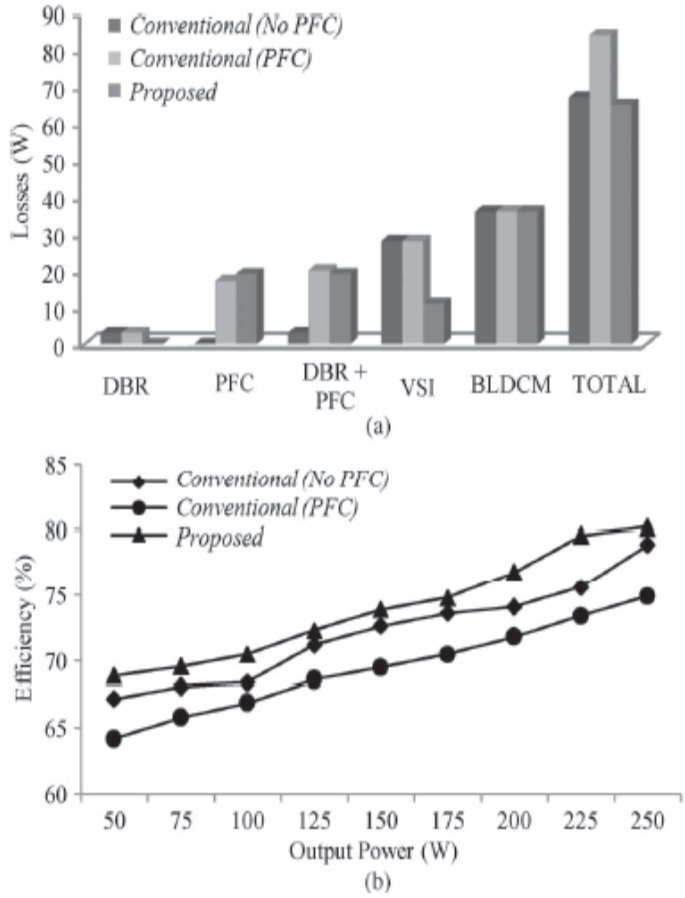


Fig. 15.Comparative analysis of (a) losses and (b) the efficiency of theconventional and the proposed configuration.Table VII shows a comparative analysis of three different configurations of the BLDC motor drive. The evaluation is based on the control requirement, sensor requirement, and losses in the PFC converter and VSI-fed BLDC motor. The proposed scheme has shown a minimum amount of sensing requirement and cost with the highest efficiency among the three configurations, and hence, it is a recommended solutionfor low-power applications.

IX. CONCLUSION

A PFC BL buck–boost converter-based VSI-fed BLDC motor drive has been proposed targeting low-power applications. A new method of speed control has been utilized by controlling the voltage at dc bus and operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor for reducing the switching losses in VSI. The front-end BL buck–boost converter has been operated in DICM for achieving an inherent power factor correction at ac mains. A satisfactoryperformance has been achieved for speed control and supply voltage variation with power quality indices within the acceptable limits of IEC 61000-3-2. Moreover, voltage and current stresses on the PFC switch have been evaluated for determining the practical application of the proposed scheme. Finally, an experimental prototype of the proposed drive has been developed to validate the performance of the proposed BLDC motor drive under speed control with improved power quality at ac mains. The proposed scheme has shown satisfactory performance, and it is a recommended solution applicable to low-power BLDC motor drives.

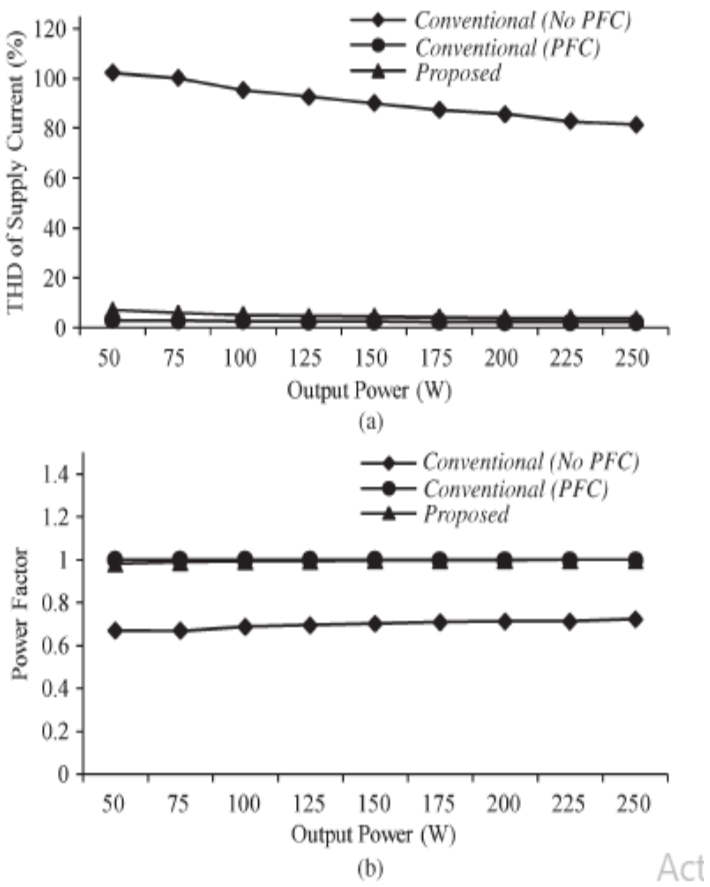


Fig. 16.Comparative analysis of (a) THD of supply current at ac mains and (b) power factor variation with output power for the conventional and the proposed configuration.

TABLE VII
COMPARATIVE ANALYSIS OF PROPOSED CONFIGURATION WITH CONVENTIONAL SCHEMES

	Conventional (No PFC)	*Conventional (PFC)*	*Proposed*
Variable DC Bus	-	No	Yes
Control (BLDC Motor)	Current Controlled (Complex)	Current Controlled (Complex)	Electronic Commutation (Simple)
Control (PFC)	-	Voltage Follower	Voltage Follower
Sensor (BLDC Motor)	2-Current + 1-Hall	2-Current + 1-Hall	1-Hall
Sensor (PFC)	-	1-Voltage	1-Voltage
Losses (DBR+ PFC)	-	Medium	Low
Losses (VSI)	High	High	Low
Efficiency	Medium	Low	High
PFC	-	Yes	Yes
Cost	Medium	High	Low

APPENDIX

BLDC Motor Rating: four poles, *Prated* (rated power) = 251.32 W, *Vrated*(rated dc link voltage) = 200 V, *Trated*(ratedtorque) = 1.2 N·m, $\omega rated$(rated speed) = 2000 r/min, *Kb* (back EMF constant) = 78 V/kr/min, *Kt*(torque constant) = 0.74 N·m/A, *Rph*(phase resistance) = 14.56 Ω, *Lph*(phaseinductance) = 25.71 mH, and *J* (moment of inertia)=1.3 × 10−4 N·m/A2.*Controller Gains:* k_p= 0.4, k_i= 3 (simulation); k_p= 0.4,k_i= 0.001 (experimental).

Dynamic Model of BLDC Motor: **A dynamic model of the** BLDC motor is developed in terms of time derivative of current, speed, and position.

The per-phase voltages (*Van*, *Vbn*, and *Vcn*) of the BLDC motor are given as [6]

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = R_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} p \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} \quad (17)$$

where*i*an, *i*bn, and *i*cn are the phase currents, *e*an, *e*bn, and *e*cn are the phase back EMFs, *Rs* is the per-phase resistance, L isthe self-inductance, M is the mutual inductance of the stator's winding of the BLDC motor, and p is the time differential operator.

The sum of the currents in three phases is zero for a threephasestar-connected BLDC motor given as

$$i_{an} + i_{bn} + i_{cn} = 0. \quad (18)$$

Now, substituting (18) in (17), the VA relation is obtained as

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = R \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix} \mathrm{p} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix}$$

Now, by rearranging (19), the current deriva tained as

$$p \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} = \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix}^{-1} \times \left(\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} - \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} - R_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{} \\ i_{} \\ i_{} \end{bmatrix}$$

The electromagnetic torque T_e is expressed as [6]

$$T_e = \frac{e_{an} i_{an} + e_{bn} i_{bn} + e_{cn} i_{cn}}{\omega_r}.$$

whereλx represents the flux, the functions $f$xn(θ) have thesame shape as that of the back EMF, and "x" and "n" represent the phase "a," "b," or "c" and neutral terminal, respectively. Now, substituting (22) into (21)

$$T_e = \lambda_a f_{an}(\theta) i_{an} + \lambda_b f_{bn}(\theta) i_{bn} + \lambda_c f_{cn}(\theta) i_{cn}.$$

The torque balance equation is expressed as [6]

$$T_e - T_l = J \frac{d\omega_r}{dt} + B\omega_r \qquad (24)$$

where$T_l$is the load torque, J is the moment of inertia of the motor, and B is the frictional constant.

By rearranging (24), the speed derivative is expressed as

$$p\omega_r = \frac{(T_e - T_l - B\omega_r)}{J}. \qquad (25)$$

The position derivative is expressed as [6]

$$\frac{d}{dt}(\theta) = \omega_r \Rightarrow p\theta = \omega_r. \qquad (26)$$

Equations (20), (25), and (26) represent the current, speed, and position derivative of the BLDC motor and, hence, the dynamic model of the BLDC motor drive. Now, at any instance of time, two switches, one each from the upper and the lower leg, remain in the "ON" state other than the switches in the same leg. As shown in Fig. 5, during the ON state of switches $S1$ and $S4$, dc link voltage Vdcis applied to line "a-b." The per-phase voltages Vao, Vbo, and Vco with respect to terminal "o" are given as [6]

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} (S_1 - S_2) \\ (S_3 - S_4) \\ (S_5 - S_6) \end{bmatrix} \begin{bmatrix} \frac{V_{dc}}{2} \end{bmatrix} \qquad (27)$$

where$S1$–$S6$ are the switching states of the VSI's switches and are replaced by "1" or "0" for the "on" and "off" positions of the switch, respectively. Table II shows the corresponding switching states and perphasevoltages with respect to terminal "o" based on the rotor position as sensed bym Hall-effect position sensors. The neutral voltage Vno, where terminals "n" and "o" are

shown in Fig. 5, is given as [8]

$$V_{no} = \frac{(V_{ao} + V_{ao} + V_{ao}) - (e_{xn} + e_{xn} + e_{xn}}{3}$$

Moreover, the phase voltages of the BLDC mot expressed as

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} (V_{ao} - V_{on}) \\ (V_{bo} - V_{on}) \\ (V_{co} - V_{on}) \end{bmatrix} = \begin{bmatrix} (V_{ao} + V_{no}) \\ (V_{bo} + V_{no}) \\ (V_{co} + V_{no}) \end{bmatrix}$$

Equation (29) is used with (27) and (28) to obtain the perphasevoltage which is finally used in (20) to determine the current derivative for obtaining the dynamic model of the BLDC motor.

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