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Optimization of VLSI Circuit Design and Implementation

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Abstract:

As a result of digital circuits, transistors can be used more easily, and devices may be constructed as switches. The introduction of the vacuum tube had a profound effect on the development of electronics, despite challenges such as high power and a hundred anode tensions. The introduction of the transistor greatly reduced power requirements in microelectronics. This laid the groundwork for future low-energy appliances. Reduced functionality and increased power per unit space have resulted from the consolidation of several functions into a single chip and the subsequent improvement in circuit performance, which has necessitated the development of more effective methods of dissipating generated heat. Their primary problem in the VLSI setting is the lack of power.

1. Introduction

Low power consumption is a hot topic in the electronics business nowadays. VLSI designers primarily think about the space, power, and speed requirements. Power dissipation is a key factor in the design of modern VLSI modules.

As design speeds and complexity continue to rise, it's clear that several strategies for reducing VLSI chip energy are needed. Growing exponentially. As a result of maximizing local and global strengths, ICs with 100 million transistors have clocked at above 1GHz in the last year. There is leakage in the many current types that facilitate power dissipation. Short channel effect caused by decrease in transistor scaling causes current to pass via parasite diodes generated between drain bulk and source mass regions. We may divide the power lost in the discharge into two categories: static power loss and kinetic energy loss. Leakage power and standby power dissipate statically. The current-based short circuit's power dissipation occurs in real time.

1 Drawback

Power Optimization

Various techniques used for testing, its application and disadvantages are shown in below

Table 1 various techniques used for testing, its application and disadvantages

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Technique	Disadvantages	Application
Test Vectors Reordering	For large set of test vectors, the CPU time needed to reorder vectors is bit high.	External Testing
Low Transition TPGs	Need a longer sequence of test vectors to get a high fault coverage.	Test-per-Scan BIST & Test-per-Clock
X-Filling	They require more test patterns to achieve a target fault coverage.	Test-per-Scan BIST
Scan Cells Reordering	Routing congestion problems during scan routing.	Test-per-Scan BIST
Test Vector Compaction	In some cases more test patterns are needed to get a target fault Coverage	Test-per-Scan BIST & Test-per-Clock
LFSR Parameter Selection	Needs huge CPU time to find the best parameters (e.g. the best seed).	Test-per-Scan BIST & Test-per-Clock
Low Power ATPG	Needs more CPU time than conventional ATPG	External Testing
Scan Architecture Modification	Hardware area overhead is significantly increased	Test-per-Scan BIST
LFSR Reseeding And Compression Techniques	Needs a moderate hardware area overhead	Test-per-Scan BIST

Power Estimation

In power estimation, simulation and probabilistic methods are used. These methods require detailed structure of the circuit and its interconnection. There is a tradeoff between accuracy and efficiency. It requires more time to implement and simulate for large circuits.

VLSI Circuits

ing networks, cars, audio instruments, toys and body implants. The technology of the Micro-Electro – Mechanical System (MEMS) facilitates the production of interdisciplinary mechanical equipment on IC, combining small scale mechanical and electronic systems. Sensors and acceleration capability for automotive airbags are, for example, installed on a chip where an accelerometer sense a rapid increase in the car speed and detects an impending crash. These developments made the ICs for common use and one of the greatest accomplishments of mankind. In these last five decades, the transistor count has grown from a few hundred to more than 20 million. The transistors are five generations. In the last decade in particular, major advances for electronic devices and mobile phones have been noted in the IC industry. This makes it very obvious in the coming decade that several Giga Hertz can be used for chip building with millions of transistors and that millions of mechanical and electrical equipment can be used for Micro Electronic mechanical chip construction. These chips will allow a new age of mobile devices that includes these applications as augmented perception, wearable and implantable computers. It will provide all people with cost-effective, regional point-to - point connectivity. The evolution of IC technology began in the 1960s with the inclusion of very few transistors (SMIS). Millions of transistors combined into one chip are actually being referred to as VLSI (Very Large Scale Integration) chips. Modern ICs were simpler and provided a few flip –flops and gateways. For a single transistor with a simple condenser network, some ICs were more intelligible for performing a logical function.

Over the last ten years, very large interface architecture has been evolving enormously with screen sizes reduced from the micrometer to the nanometer. The rule of Moore notes that every 1.5 years the cumulative transistors on a single integrated circuit increase. The transfer ranges of several hundred transistors per circuit to the several millions of transistors per day per single chip. Only by reducing the feature sizes of the integrated circuit is this significant migration possible. The practical sizes were changed from only a few meters to only a few nanometers. In order to achieve high device efficiency, electronic design automation (EDA), due to the growing difficulty of modern VLSI chip design, plays a significant role. The architectural planning process for VLSI includes partitioning, floor planning, arranging, routing and compacting. The big increase in VLSI circuits will in future depend upon

Computers for processors, RAM, control module, etc. use embedded modules. ICs often refer to switching mechanisms, messaging platforms, comput

the advancement of resources for physical system automation.

2. Review of literature

Arkadiy et al (2014) in 2002, it was proposed that the Gate Diffusion Input (GDI) technique reduce the area and power of digital VLSI circuits. For twin-well, silicone on Insulator (SOI) methods, the GDI logic was initially proposed. It allowed the implementation with just two transistors of a wide range of difficult logical functions. This arrangement was suitable for the design of regular digital circuits which had a much smaller area than existing PTL and Static CMOS methods, while improving power. In addition, GDI circuits were affected by a reduced swing due to threshold declines as were PTL implementations. Conversely, despite the need for swing restoration circuits, the logical flexibility and transistor count of the GDI cell have decreased substantially.

T. Suguna and M. Janaki Rani (2018) Because the power demand is reduced, CMOS is the key component in designing VLSI devices. Power optimization in deep submicron CMOS technologies has become an overridden concern. As the computer is smaller, the key problems are power usage cuts and in general power conservation on the processor. Power management is critical for many designs in order to reduce package expenses and prolong battery life. The leakage of control management also has a big role in the overall power dissipation of VLSI circuits. This essay seeks to clarify the advancements and advances in the area of power management in deep submicron regions of CMOS circuits. This survey was useful for the designer to choose an appropriate technology according to the requirement.

The authors in **Tennakoon and Sechen (2012)** suggested an effective gate-sizing technique for lagrangian relaxation with clear constraints. However, the methodology requires the practical harmonization of a good initial solution and sub gradient optimization.

The authors in **Berkelium and Jess (2013)** proposed a flexible linear programming system for gate size in a bid to increase code sophistication without substantial effect on solution consistency. Secondly, two popular methods for improving circuit performance are buffer insertion and wiring in the context of increasing wire delay. The retardation of a net depends on the wire resistance and capacity product directly.

Ambily Babu (2014) Designers have been finding ways to speed up automated circuits and the field of design since the advent of the First IC. Advances in VLSI manufacturing technologies recently allowed the complete Device to be mounted on a chip. The drawback was that the power dissipation of modern VLSI is a crucial parameter. This paper provides insight into specific energy dissipation sources in digital CMOS and the technologies for circuit and system power optimization.

Duan et al. (2009) Suggesting a technique of bus encoding using prohibited cross-talk reduction transitional free algorithm for on chip interconnection with the VLSI. A version of the binary Fibonacci number method was introduced as mapping and coding method. The mathematical analysis showed that the Fibonacci Numeral System (FSN) can represent all numbers through Forbidden Transition Free (FTF) vectors which reduced the crosstalk delay and remedied the procedure in which the free binary Fibonacci coding words are generated.

M. Sivakumar and S. Omkumar (2017) Optimizations at different design stage stages, such as algorithms, software, logic and circuit & process technologies, are needed to achieve a reduction in power consumption. This paper looks at the two logic solutions for software architecture with low capacity. For raising the switching operation capacity of individual logic gates, optimization strategies are performed. The power may be that by optimizing the circuit or minimizing the logical stage. Within this paper we pursue the method of circuit level optimization to every the region and strength. The proposed asynchronous parallel self-time adder (PASTA) technology uses modified Gate Diffusion Input (GDI) logic. In the same way, the XOR gate and half adder structure is reduced to a low surface and a low energy material. "The digital circuit is centered on the multi-value principle by growing the representation domain from the two rates (N=2) to N>2. The key benefit of this method is compensating for the inability to enforce the uniform series of MVL gates on current built-in circuits. The proposed Adder GDL logic provides fewer transistors (area) and low power consumption from the tests than the current technology. The proposed MVL technology facilitates the construction of a digital MVL circuit package to obtain binary circuit values. The simulation phase is carried out by the device tanner14.11 to test the reliability of the PASTA & MVL circuits, while having little power and limited wiring delays relative to binary and three-value Logic.

Coello (2011) Emphasizes multi-objectify optimization through evolutionary theory and describes the numerous approaches utilizing this approach. The author notes, for optimizing VLSI circuits by weighted summation that the additional

goal functions may be used to generate a single feature. In particular, the author demonstrated in Vector Evaluated Genetic Search (GS), the modified version of conventional GS during the selection step, the effectiveness of some combination circuits and multiplier – free IIR filters.

Kumar et al., (2010) have also discussed a strategy to recognize in a fully specified set of vectors the don't care locations, keeping in mind both fault activation path and fault propagation path, which is based on PSO for vector reordering. Cellular Automata (CA) is a powerful computing and modeling tool in which the cell is updated at every clock cycle. The state of the cell is dictated by the immediate neighbors, typically termed as two states-three neighborhoods CA. Use of CA has been reported in literature for testing of the VLSI circuits. Transistor width, door scale, and cable size problems are important to VLSI architecture as they may allow choices between the different priorities of the cost feature. In **Fishburn and Dunlop (2015)**, TILOS uses an iterative transistor sizing technique based on convex programming based on the sensitivity of critical delays to enhance performance. The advantage of TILOS is that a local optimum is global is the use of convex delay models for transistor size. The iterative approach has been further improved. Nonetheless, for issues of more than a few thousand broad parts, the general approach does not work.

Ehrgott and Gandibleux (2012) Details of advanced MOP resolution are described, including Fuzzy approaches, digital methods and developmental algorithms. Multi-target optimization strategies are used for the configuration of analog and digital circuits. Multilateral optimization is a central research subject in science and engineering. A number of videos, review papers and even textbooks on this topic are published. Various aspects are defined of non-linear multi-target optimization.

Sellathamby et al., (2005) Suggested BIST low power output. Transitions are minimized in their function by growing the distance between the following bits in the test sequence, carried out using updated LFSR. The findings of the simulation indicate that the power dispersion with adjusted LFSR is that. Have launched the latest TPG with a decreased power dissipation that is more suited for BIST systems without impacting fault cover. The patterns generated by a counter and a gray code generator are XOR-end with the low power seed LFSR. The result shows significant testing power reduction with the proposed method. To test the VLSI Modules, LFSR is an important part of BIST to generate the patterns for the testing. Many researchers have worked on the low power techniques for LFSRs and counters.

Van Ginneken (2010) presented an optimum buffer insertion algorithm based on dynamic programming. The number of buffer sites that were the foundation for several subsequent studies on net buffer deployment has a quadratic complexity. Thanks to its variations, it is correctly measured by adjusting the processor voltage and fixing timing errors. In contrast to worse housing and mathematical optimization, the Razor platform eliminates the requirement for voltage margins and thus a large overhead economy.

Kapil Mangla and Shashank Saxena (2015) in day today life, Product Chip Systems (SoC) are required. The SoC is named as millions of chips in one slot. These million chips are integrated into the single chip by decreasing each chip's transistor size. This CMOS technique can therefore be used in the SoC product. CSLA is mainly used to reduce the size of the chip and raising the gap of propagation. The asynchronous automatic parallel adder (PASTA) works by it erotic coding. Therefore, this adder removes the number of unwanted clock cycle activation to achieve high speed and low power.

Lundstrom (2007) Rapid technical growth has a major influence on engineering progress. The technical advancement allows innovative and better computer devices to be produced, thus promoting the growth of several innovation fields. The need for high accuracy and efficiency is greater than ever before for multi-functional tablets, cameras and laptops. Besides conventional efficiency improvements, customers are involved in battery life, durability and renewable computing. Multi-functional characteristics, a high performance with low resources, compact and concurrently cost effective are the main objectives of designing these goods. A common method to accomplish these objectives is the measurements of the fundamental elements of the circuit. Thanks to growing

Leakage energy and durability issues, the shift to lower technology generations for high efficiency and denser application are getting more complicated. Therefore, the backward progression of production approaches the boundaries of ballistic transport.

Den nard et al (2018) the development in VLSI technologies has shaped the analog and digital circuits to scale down into nanometer range, the concern regarding power consumption has increased speedily due to the structure density and the design complication. Thus, there exists a prerequisite of a precise power modeling technique to direct the problems of nanometer processing technologies. In this paper several modeling techniques have been discussed and the process of Input Vector Control (IVC) is found to be a preferable substitute in getting the low power consumption. IVC design is built on the effect of transistor stacking. It is extremely

preferred due of its nature of independency on the other technological parameters.

Gary Yeap (2008) we identified various leakage and static current reduction strategies, voltage switching, capacitance, frequency switching and noticed a variety of the common low power architecture merits. The criteria for low power architecture were described by Sung-mo Kang et al, (2013), and different methodologies were proposed for low power consumption. The key emphasis of this chapter was the circuit – or transistor architecture.

Geetha et al (2017) the key challenge for late hardware companies is low strength. Control dispersion is an essential idea for VLSI Chip outline in terms of execution and area. Check management procedures are mainly used for low power circuits and frameworks configuration. Results show that the transistor leakage accounts for 40 per cent or significantly higher aggregate power utilization. This rate would rise with the rise in creativity if rationalization strategies do not add leakage within containment points. This paper focuses on the enhancement of circuits and designs mechanization techniques to achieve this aim. The paper also outlines various problems with the circuit boundaries at structure, legal and device rates and offers specific approaches to resolve the abovementioned problems. The initial part of the paper provides a schedule for primary sources of CMOS transistor leakage current.

The second section of the paper reveals several strategies for simplifying the device to change the current standby leakage. Some current procedures, like rest, stacking and reading strategies, are discussed for CMOS entrance planning that essentially reduces leakage streams. This paper discusses the benefits of the reader approach because there is no extra monitoring and hardware evaluation, thereby limiting the range increase and additionally, as opposed to other device, the power dissipation in dynamic state and not impacting the dynamic capacity that is the main disadvantage of other leaking reduction techniques.

Kamal K Mehta, (2016) The literature review discussed the issue of dynamic power dissipation and the associated technological question. And different factors have been established to reduce the dissipation of electricity. This paper addresses the residual impact in the architecture of the device after integrating complex power problems. Mr Suhas D. Mr Suhas D. The various lower energy architecture approaches were suggested by caked et al (2016). And the various factors to reduce switching activities were also provided. And also it noticed that the usage of advance technologies minimized swing or operation approaches to low power interconnections.

Rohit Lorenzo & Saurabh Chaudhury (2017) An ever rising demand has resulted in aggressive scaling of portable and batteryoperated systems. While scaling technology enables quicker and high performance products, it induces excessive power dissipation, in particular leakage. The power dissipation of leaks is now a key factor in today's high performance chip's total energy usage. Many who have introduced many creative strategies to create low-performance circuits and systems have a tremendous need to reduce the dissipation of power in high-density chips. Nano-scale VLSI chips have ultra-thin gate oxide, very low threshold voltage and narrow channels. The VLSI chips are very tightly optimized. The most challenging problem in VLSI circuits and devices was thus leakage control dissipation. In this article, we provide a summary of the cutting-edge strategies for reducing leakage rates Since 1995. This also classifies the different leakage minimization methods conceptually. In addition, a thorough study has been carried out using a simple metal oxide semiconductor (CMOS) gate with the SPICE method for the influence of development nodes on leakage and distance. It also checks for process, voltage and temperature variations in relation to reliability issues. This detailed research along with the experimental findings will be used to pick the most successful approach to minimize leakage.

3. Conclusion and future work

When compared to the conventional Domino mapping method, the cell re-ordering based mapping strategy introduced in Chapter 4 provided a substantial latency benefit. The space lost as a result of rearranging cells is also minimized. In particular, this method optimizes the layout for high-performance uses. A comparison of the transistor count between the suggested decomposition-based technique and the static CMOS logic style shows that the latter has a lower threshold for implementation. An analogy between mixed CMOS circuits and just dynamic and solely non-dynamic actualizations based on the literature cited elsewhere. Additionally, it is possible to draw the conclusion that mixed CMOS circuits are ideal for high-speed and low-power applications such portable digital devices, mobiles, etc. Using the suggested pattern recognition based clock gating technique, significant power savings were seen. This chapter devotes extensive attention to the clock signal, which plays a crucial role in the Domino block. The result was a design that was competitive with other low-power methods in the

literature. This bodes well for the design's potential use in a wide variety of portable device types.

Incompletely stated Boolean functions may be accommodated by further generalizing the decomposition techniques. However, there are still many questions unanswered and challenges to solve, thus there is room to expand this study. For the sake of the raw mapping method, we may assume that the gates are either "and" or "or" logic. The basic mapping circuit may be expanded to include additional features, and rules for combining them can be generated in the same way. It is also possible to use ideas like the average case delay in terms of incompletely specified Boolean functions and the application of logical effort to estimate the delay. The best candidate may be selected from the Pareto optimal front, among other multi-objective optimization methods. Our method reduces the amount of switching power and space required by the clock gating logic. However, the gating logic considerably affects the delay of the circuit. Consequently, the performance metric may be included into the study.

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