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DESIGN AND ANALYSIS OF NOVEL 1-BIT HYBRID FULL ADDER AT 90NM AND 180NM TECHNOLOGY

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ABSTRACT
It is reported that a 1-bit complete adder can be implemented using a combination of complementary metal-oxide-semiconductor (CMOS) and transmission gate logic. The original design was built for 1 bit, and afterwards support for 32 bit was added. Cadence Virtuoso tools were used to realise the circuit in 180 and 90 nm technologies. Power, delay, and layout area were measured and compared to similar current systems, including gearbox gate adders, gearbox function adders, hybrid pass-logic with static CMOS output drive complete adders, and complementary pass-transistor logic. The deliberate use of very weak CMOS inverters coupled with strong transmission gates resulted in an extraordinarily low average power consumption (4.232 W) and a relatively low latency (226 ps) for a 1.8-V supply at 180-nm technology. At 1.2 V supply voltage and 90 nm technology, the corresponding values were 1.1965 W and 98 ps. It was determined that the current solution significantly outperforms the existing full adder designs in terms of both power and speed.

I. INTRODUCTION

Integration of several different circuits using transistors onto a single chip is known as very large scale integration (VLSI). The development of very large scale integration (VLSI) began in the 1970s, with other advanced semiconductor and communication technologies. A very large scale integration device (VLSI) chip. As chips have become increasingly complex, with thousands of individual transistors, the word has become less commonplace.

1.1 OVERVIEW

Each semiconductor's primary component was a single transistor. Subsequent advancements included an increase in transistor count, which allowed for the incorporation of a wider variety of specialised features and systems. In the past, integrated circuits were made up of only a few devices, perhaps as many as ten diodes, transistors, resistors, and capacitors, making it possible to produce one or more logical doors on a single device. The advancements in procedure that brought about the devices with multiple rational entryways currently reflectively known as "little scale joining" (SSI) encouraged the development of large scale incorporation (LSI), i.e., frameworks with at least a thousand rational entryways. Modern technology has greatly beyond this template, and chips now feature countless individual transistors and millions of gates.

There was once an effort to classify and fine-tune the various forms of large-scale integration that go beyond VLSI. We used phrases like "Ultra-substantial-scale Integration" (ULSI). However, the vast array of ports and transistors on common devices has made such nitpicking moot.

The use of terms implying integration levels greater than VLSI has largely died off. As a matter of fact, even VLSI is currently somewhat intriguing, considering the common belief that all chips are VLSI or superior.

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1.2 MOTIVATION

Any digital system, digital signal processing system, or control system relies heavily on the addition operation. The efficiency and reliability of a digital system depend heavily on the quality of its on-board adders. Since subtractions, multiplications, and divisions are also performed digitally, adders are an integral part of most computer systems. We can improve the system's efficiency by using adders in a more effective manner. As aspiring engineers, we are motivated by a desire to improve the state of the art for future generations. That's why we're looking into adders to see where we can make improvements to the system's speed, power, and footprint.

1.3 WHAT IS VLSI?

"Very Large Scale Integration" is the abbreviation for VLSI. This is the area of study concerned with cramming ever more logic devices into ever less space.Very Large Scale Integration (VLSI) is the concentration of a large number of transistors on a single silicon chip.

Modified semiconductor material allows for the design and manufacture of highly miniature and complicated electronic circuits.

Each transistor on an integrated circuit (IC) is only a few millimetres in size, but ICs are used in virtually all electronic logic devices.

1.3.1 HISTORY OF SCALE INTEGRATION

First integrated circuit (JK-FF, created by Jack Kilby at TI in the late 1950s) Early 1960s Small-scale integration (SSI)

Medium Scale Integration (MSI) in the late 1960s—tens of transistors on a single chip

10,000 transistors on a chip in the 1980s; 100,000 transistors in the 1990s; 1,000,000 transistors in the 2010s; Ultra LSI is occasionally used for 1,000,000 transistors on a chip.

Scaled-Down Integration (from 0 to 102) - SSI

Medium-Scale Integration (MSI) (Pages 102-103).

Large-Scale Integration (LSI) (Page(s):(103-105)

"Very Large Scale Integration" (or VLSI) (pp. 105-107)

ULSI, or Ultra Large-Scale Integration (>=107), means exactly that.

1.3.2 ADVANTAGES OF ICS OVER DISCRETE COMPONENTS

While our focus will be on ICs, it is important to note that the attributes of ICs (what can and cannot be efficiently put in an IC) heavily influence the design of the overall system. There are many essential ways in which integrated circuits enhance system features. There are three main benefits of ICs compared to discrete component digital circuits:

- Dimensions: Transistors and wires in integrated circuits are often measured in micrometres rather than the millimetres or centimetres used for discrete components. Since smaller components have less parasitic resistances, capacitances, and inductances, they are faster and use less power than their larger counterparts.
- Rapidity: Changing a signal from logic 0 to logic 1 within a semiconductor is substantially faster than doing it between chips. Inter-chip communication can be hundreds of times slower than intra-chip communication, yet intra-chip communication can occur on a printed circuit board. Smaller components and connections mean less signal slowing parasitic capacitance, which is why on-chip circuitry can operate at such fast speeds.
- In-chip logic processes also require significantly less power. Again, smaller circuits on the chip are mostly responsible for the reduced power consumption; their lower power requirements are a result of smaller parasitic capacitances and resistances.

1.3.3 VLSI AND SYSTEMS

The benefits of integrated circuits extend to the whole system because of these features.

• Less bulky in appearance. Consider the benefits of handheld mobile phones and other small electronic devices.

Reduced energy needs. When several common components are combined onto a single chip, power consumption drops dramatically. A smaller, less expensive power supply can be utilised; less power consumption equals less heat, thus a fan may no longer be needed; and a simpler cabinet with less shielding for electromagnetic shielding may be conceivable, all because of the reduction in power consumption.

• Lower price. The price of a system can be lowered by cutting down on its complexity by eliminating unnecessary parts, supplies, cabinets, etc. Although custom integrated circuits (ICs) are often more expensive than the conventional components they replace, the knock-on effects of integration can reduce the overall system cost.

Both the technology of IC production and the economics of ICs and digital systems are necessary for an understanding of why IC technology has such a deep influence on the design of digital systems.

APPLICATIONS

- The electronic components of vehicles.
- VCRs are operated by digital electronics.
- Money Transfer Service, or ATM
- Computers, both home and office-based
- Electronic health records, etc.

1.3.4 APPLICATIONS OF VLSI

These days, we rely on electronic technologies for pretty much everything. Mechanisms that once functioned mechanically, hydraulically, or in some other way have sometimes been replaced by electronic systems,

which are typically smaller, more flexible, and easier to service. Sometimes, though, electronic systems have given rise to whole novel uses. Some of the functions of electronic systems are more obvious than others.

• Portable media devices (MP3 players) and DVD players need surprisingly little power to execute complex algorithms.

• The car's electronic systems are responsible for its sound and display features, as well as its fuel injection, suspension, and anti-lock braking (ABS) system controls.

• On-the-fly video compression and decompression at high resolution data rates are made possible by digital electronics in consumer devices.

• Despite their specialised purpose, even low-cost terminals for Web browsing require complex electronics.

Word processing, financial analysis, and video gaming are all possible on today's desktop and laptop computers. Computers have both general-purpose hardware, such as a central processing unit (CPU), and specialised hardware, such as hardware designed to speed up disc access or display.

• Medical electronic systems monitor internal processes and issue alerts based on advanced processing algorithms. Rather than overwhelming customers, the availability of these complex systems merely generates demand for even more complicated systems.

Integrated circuits and electronic systems are becoming increasingly difficult to design and manufacture as a result of the increasing intricacy of their intended applications. As systems get more complex, we develop not a handful of general-purpose computers but an ever-expanding spectrum of special-purpose systems, which is perhaps the most remarkable aspect of this collection of systems. Our success in doing so is indicative of our rising competence in integrated circuit production and design, but the ever-increasing requirements of our clients continue to push us to the brink of our capabilities.

II. LITERATURE SURVEY

Power-efficient VLSI and ultra large-scale integration (ULSI) designs are in high demand because of the proliferation of battery-operated mobile devices such as cellphones, PDAs, and laptops. One of the most essential building elements of all these circuit applications is the full adder, hence it has been a central area of study for many years [1, 2]. Implementing 1-bit full adder cells was studied using a variety of logic approaches [3]-[11], each with its own set of benefits and drawbacks. The reported designs can be roughly sorted into two groups: 1) static styles, and 2) dynamic styles. Static full adders are preferred over their dynamic counterparts because they are more stable, consume less power, and take up more room on the chip.

There is a trade-off in performance between the various logic styles. Transmission gate full adder (TGA) [7], [8], and static complementary metal-oxide-semiconductor (CMOS) [3], as well as complementary pass-transistor logic (CPL) [5], [6], and dynamic CMOS logic [4] are the most important logic design types in the conventional domain. Hybrid-logic design style [9] describes the various adder designs that combine several types of logic.The full adder's performance is enhanced by these designs because they take advantage of the benefits offered by various logic techniques.

Standard complementary (CMOS) style-based adders (with 28 transistors) have a high input capacitance and need buffers [3, but they are resilient against voltage scaling and transistor sizing). The mirror adder [4] is a smart design of a complementary type that uses nearly the same amount of power and transistors as the adder [3], but has a shorter maximum carry propagation path/delay inside the adder than a regular CMOS full adder.CPL, on the other hand, uses 32 transistors to effectively restore voltage swings [5, 6]. However, CPL is not a good option when power consumption is little. The technique is limited by issues including large transistor count, static inverters, and input overloading due to the high switching activity of intermediary nodes (increased switching power). TGA, which needs only 20 transistors for full adder implementation [7], [8], successfully addresses the primary problem of CPL, namely, the voltage degradation. Researchers are nonetheless worried about other issues with CPL, such as its limited speed and high power requirements.Later, scientists concentrated on the hybrid logic method, which leveraged the strengths of many logic types to boost performance. Vesterbacka [10] described a 14-transistor complete adder that used many logic techniques. Similarly, Zhang et al. [11] suggested a complete adder that uses hybrid pass logic with static CMOS output drive (HPSC). Using a single transistor logic module and just six transistors, this HPSC circuit generates XOR and XNOR operations simultaneously, and then uses a CMOS module to generate the full swing outputs of a complete adder, although at the expense of increased transistor count and reduced speed. However, most of these hybrid logic adders have a problem with weak driving capabilities, and their performance drops dramatically in the cascaded mode of operation if the appropriately designed buffers are not included, so the hybrid logic types only offer limited promise.

The primary goal of this article is to enhance the existing full adder by reducing its power consumption, latency, and transistor count. The circuit was realised with Cadence Virtuoso tools at both the 180-nm and 90-nm node levels. By incorporating very weak CMOS inverters

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together with robust transmission gates for 1.8 V supply, the suggested circuit's average power usage (4.1563 W) was drastically lowered when implemented at 180-nm technology. However, with 180-nm technology, the layout area (excluding buffer) was equivalent to previous hybridised implementations and the delay of the circuit (224 ps) was better than other full CMOS implementations. The average power consumption, latency, and layout area (without the buffer) for 90-nm technology running on a 1.2-V power supply are 1.17664 W, 91.3 ps, and 25.84 m2, respectively. The design for a 32-bit carry propagation adder was validated, and it was found to be effective.

III. EXISTING SYSTEM

3.1 ADDERS

If you can count to five, you can control anything. Any digital system, digital signal processing system, or control system relies heavily on the addition operation. The efficiency and reliability of a digital system depend heavily on the quality of its on-board adders. Because of their widespread application in other fundamental digital operations like subtraction, multiplication, and division, adders are also an essential part of digital systems. As a result, increasing the speed of the digital adder would considerably improve the time it takes for a circuit made up of such blocks to complete a binary operation. A digital circuit block's efficiency is evaluated by measuring its power consumption, physical size, and processing speed.

3.1.1 Basic Adder Unit

The addition of two binary numbers, or bits, is the simplest form of arithmetic. A half adder is a combinational circuit that adds two bits using the method described below. A complete adder processes three bits at once, with the result of one addition providing the third. Using two half adders is one implementation option for a full adder. All of the adders in this study use the full adder as their fundamental arithmetic building block.

3.1.2 Half Adder

Two binary digits, A and B, can be added together with the use of a half adder. Co, the matching carry, is generated along with S, the sum of A and B. Half adders aren't very helpful on their own, but they're a great building block for more complex adding circuits (FA). Figure.2.1 depicts a proposed implementation that uses two AND gates, two inverters, and an OR gate in place of an XOR gate.

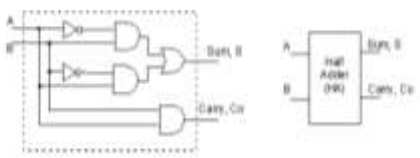

Figure 3.1: Block diagrams and logic for half-adding

Table 3.1 Half adder truth table

A	B	S	C_o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Equations:

$S = A \oplus B = A'B + AB'$

$Co = AB$

3.1.3 Full Adder

Adding three bits (A, B, and C) together with a carry in (Fig. 4.8.a) from the preceding addition is the job of a complete adder, a combinational circuit. In the same way that the half adder generates the equivalent sum S and a carry out Co, the full adder does the same. As was previously mentioned, a complete adder can be built by connecting two half adders in series, as shown in Figure 2.2b.

A second half adder receives the sum of A and B and combines it with the carry in C (from an earlier addition operation) to get the final sum S. Co, the carry, is the ORed result of the carry outs from both half adders. Both gate-level and transistor-level adders with varying performances have been described in the literature.

Boolean Equations:

$S = C \oplus (A \oplus B)$

$Co = AB + C(A \oplus B)$

Table 3.2 Full Adder Truth Table

A	B	C	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

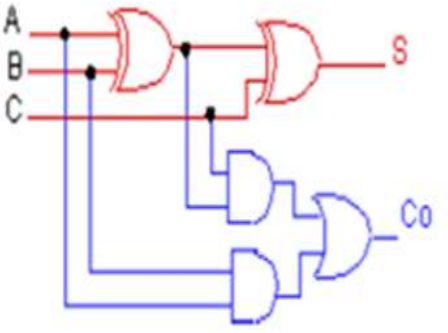

Figure 3.2a Full Adder

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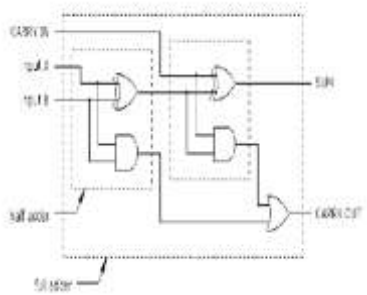

Figure 3.2b Combination full adder based on the use of two half adders

3.2 CONVENTIONAL CMOS FULL ADDER

Figures 3.1 and 3.2 depict the gate level implementation of a typical CMOS full adder cell and a 28-transistor full adder. There are 28 transistors in a 1-bit complete adder cell. For complex gates with huge fan-ins, the CMOS design style is inefficient in terms of floor space. Therefore, caution is required while choosing a static logic style to actualize a logic function. Pseudo NMOS is an easy method to implement. It is well knowledge that certain logic circuits, such as multiplexers and XOR-based circuits like adders, can be implemented using pass transistors. Regular CMOS structure with typical pull-up and pull-down transistors offering full swing output and good driving capabilities is the basis of the classic design of the standard static CMOS full adder.

Taking the logic equation and translating it directly into a complementary CMOS circuit is one technique to create the entire adder circuit. It is possible to reduce the number of transistors by using certain logical operations. It is helpful, for instance, to share some logic across the sum and carry creation sub circuits, so long as doing so does not slow down the carry generation, which is the most crucial component. Here is an example of a rearranged set of equations:

$$CARRY = A.B + B.Cin + A.Cin$$

$$SUM = A.B.Cin + CARRY(A + B + Cin)$$

It's simple to check if the new equations are equivalent to the old ones. You'll need 28 transistors for this. This circuit not only takes up a lot of room, but it also moves at a glacial pace.

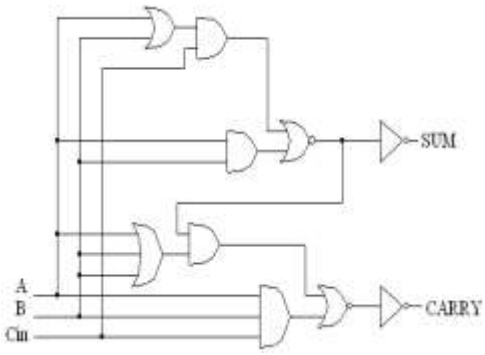

Fig 3.3: The entire adder is implemented using 28 transistors at the gate level.

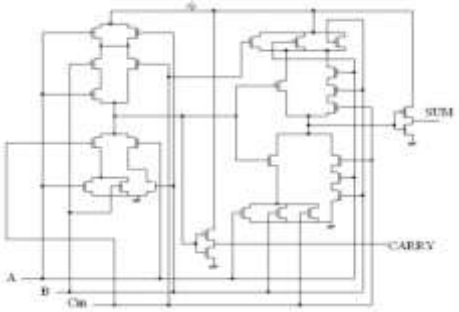

Fig 3.4: The entire adder is implemented in CMOS using 28 transistors.

3.3 TRANSMISSION GATE FULL ADDER

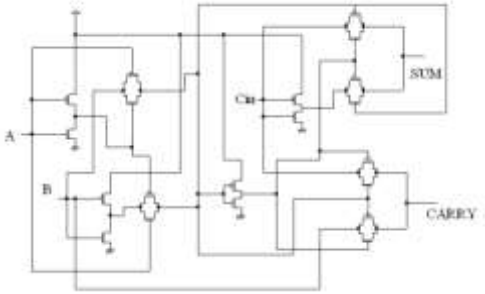

Fig 3.5: Full Adder Transmission Gate Architecture

Fig. 3.3 depicts the structure of a gearbox gate full adder, which has the benefit of producing sum and carry buffered outputs with the correct polarity but the drawback of requiring a lot of power.

Working principle: Two inverters are followed by two transmission gates that perform the function of an 8-T XOR in this circuit. After that comes the 8-T XNOR circuit board. Both Cin and Cin bar are multiplexed under the supervision of (a b) and (a b) to produce the final sum.Multiplexing a and Cin, which is modulated by (a b), allows for the computation of the Cout.

Advantage: As far as we know, it's the quickest adder ever documented. The circuit is easier to implement than a standard adder.

Disadvantage: This circuit's power consumption is higher than that of a 28T adder. However, it is more effective while using the same amount of electricity.

3.4. 14T FULL ADDER CIRCUIT

The whole adder has 14 transistors, including a multiplexer for sum and Cout signals based on transmission gates, an inverter, and two transmission gate designs. The conventional full adder's high transistor count was reduced by using XOR and XNOR circuits built on pass transistor logic, leading to the construction of a 14T full adder (see fig). When compared to earlier studies in full adders, the 14T full adder's development yielded superior delay and power consumption outcomes.

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The high-performance, low-power-dissipation multipliers went well with the 14T full adder. The threshold power loss, however, was not improved by the adder. In addition, the power requirements of the 14T adder are far higher than those of the 28T complete adder that has been demonstrated. The 14-transistor (14T) adder is faster and uses much less power (on the order of microwatts) than its 10-transistor counterpart. In comparison to adders with 28 transistors, the 14T version's threshold loss problem is much less of an issue.

Here, a MOSFET-based design for a 14-transistor full-adder circuit is shown, with the goal of enhancing the adder's performance in terms of power consumption and leakage. The 4T XOR gate is used to build this cellular automaton. It's the foundation of an adder cell, the thing that actually does the adding. It functions as though it were a single adder cell. We incorporated a pair of 4T XOR gates into the 14T complete adder cell. In the past, an XOR gate required 8 MOSFETs for reliable operation. However, modern alternatives exist.

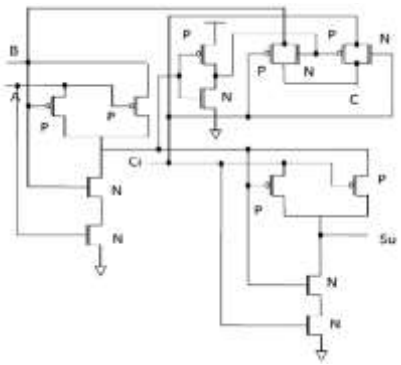

Fig. 3.6. The whole adder circuit for a 14-tuple

To accomplish this, a 4T XOR gate has been incorporated into the design. By utilising this XOR gate, the size of the entire adder can be decreased, and the overall leakage can be minimised. The figure depicts the output waveform of a 14-transistor full adder.

In addition to the inverter and the two transmission gate–based multiplexer designs for the sum and Cout signals, the 14T full adder also includes the 4T PTL XOR gate depicted in Figure. The XOR logic of these four transistors is inverted in the next stage to create the XNOR logic. Sum and Cout are both calculated using these XOR and XNOR operations in tandem. One may say that it is an expedited calculator. The circuit is less complicated than a standard adder. This circuit's power consumption is higher than that of a 28T adder. However, it is more effective while using the same amount of electricity.

Working principle: This 4-transistor XOR circuit inverts to an XNOR at the next stage. Both sum and cout are created using XOR and XNOR at the same time. Both (a xor b) and (a b) can be used to regulate the multiplexed cin and cinbar signals. Similarly, by multiplexing a and cin under the direction of (a b), the cout can be determined.

Advantage: As far as we know, it's the quickest adder ever documented. The circuit is easier to implement than a standard adder.

Disadvantage: This circuit's power consumption is higher than that of a 28T adder. However, it is more effective while using the same amount of electricity.

3.5. MIRROR ADDER

Symmetry between the nmos and pmos chains can be found everywhere. Carry generation circuits typically consist of no more than two series-connected transistors.

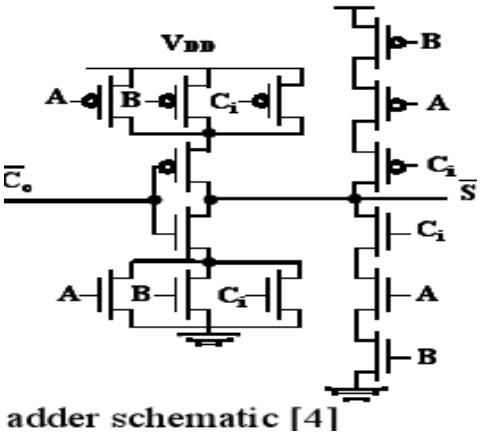

Fig. 3.7. Plan view of the Mirror Adder

The reduction of node capacitances is the primary concern during cell layout. Capacitances at the nodes of a stack can be minimised by using cout shared diffusions. Transistors wired to cin are located near the signal's final destination.

For maximum velocity, just the carry stage transistors need to be fine-tuned. Miniature transistors can be used throughout the summing stage.

IV. PROPOSED SYSTEM

In Fig. 1(a), the three blocks indicate the proposed entire adder circuit. The sum signal (SUM) is produced by XNOR modules 1 and 2, whereas the carry signal (Cout) is produced by module 3. Power, delay, and area are all carefully considered when designing each module for the adder circuit. An in-depth analysis of these parts follows.

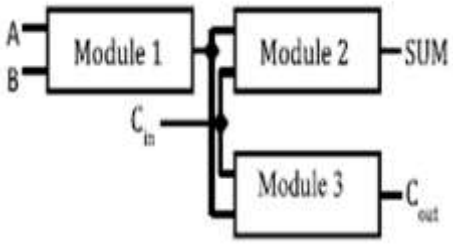

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Fig. 4.1. The Proposed Full Adder, Shown as a Block Diagram

4.1 MODIFIED XNOR MODULE

The XNOR module accounts for the vast majority of the adder's total power consumption in the proposed full adder circuit. As a result, this module was developed to consume as little power as possible while preventing voltage drop. By forming a weak inverter (with transistors having narrow channels), as shown in Fig. 1(b), the power consumption of the improved XNOR circuit is drastically decreased.

The output signals' levels can vary freely because level restoring transistors Mp3 and Mn3 are used [Fig. 1(b)]. Numerous XOR/XNOR architectures have been documented previously ([7], [12–14]). Four transistors are used in the XOR/XNOR described in [12–14], although this comes at the expense of a small logic swing. However, in contrast to the 4 T XOR/XNOR published in [12–14], the 6 T XOR/XNOR presented in [7] requires more transistors to achieve a larger logic swing. Similar to the 6 T XOR/XNOR [7], the XNOR module in this study uses 6 T, but the transistor layout is different. This study presents a modified XNOR that, in comparison to a 6 T XOR/XNOR [7], is both low-power and high-speed (with acceptable logic swing).

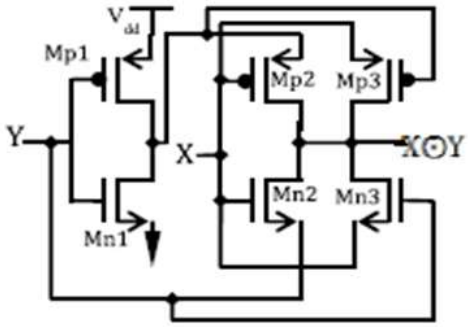

Fig. 4.2. Modified xnor module: a block diagram

4.2. CARRY GENERATION MODULE

As can be seen in Fig. 1(c), the proposed circuit uses transistors Mp7, Mp8, Mn7, and Mn8 to execute the output carry signal. One transmission gate (Mn7 and Mp7) is all that stands between the input carry signal (Cin) and its destination. Carry signal propagation delays were further reduced thanks to the employment of robust transmission gates (the channel width of transistors Mn7, Mp7, Mn8, and Mn8 was made big).

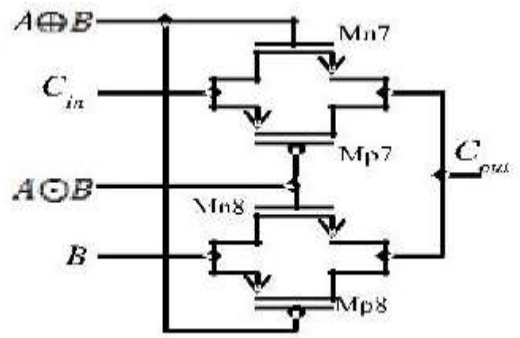

Fig.4.3. Carry generation module schematic

4.3. OPERATION OF THE PROPOSED FULL ADDER WITH SIMULATION TEST BENCH SETUP

The whole adder's intricate diagram is depicted in Fig. 2. In order to implement the whole adder's sum output, XNOR modules are used. By employing the output B' from the inverter made up of Mp1 and Mn1 transistors, the controlled inverter made up of Mp2 and Mn2 transistors may be efficiently designed. This regulated inverter produces an output that is equivalent to the XNOR of A and B. Two pass transistors Mp3 and Mn3 were used to fix the voltage drop they were causing. The whole SUM function is implemented by realising the second stage of an XNOR module using pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6). The necessary conditions for Cout generation have been deduced by analysing the truth table of a fulladder as follows:

If, A = B, then Cout = B; else Cout = Cin

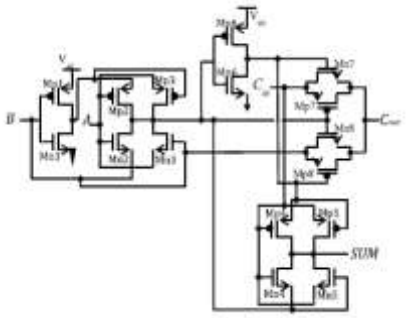

Fig.4.4. Extensive Adder Circuit Diagram

A B function verifies the inputs' A and B parity. Cout is equivalent to B if and only if transistors Mp8 and Mn8 are used to realise a transmission gate. Otherwise, a second transmission gate, made up of transistors Mp7 and Mn7, reflects the input carry signal (Cin) as Cout.

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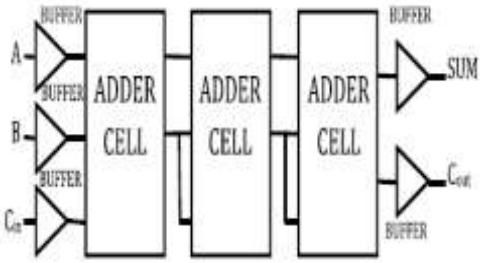

Fig4.5. Establishment of a Mock-Up Test Bench

It's possible that a single-bit adder cell's optimal performance will suffer when it's put into real-time use. This is because, in a cascaded configuration, the input signal level from the driver adder cells to the driven cells may be incorrect. Under low supply voltages, the cumulative signal degradation could cause faulty output, and the circuit could fail.A realistic simulation environment, depicted in Fig. 3, is set up to evaluate the performance of the proposed complete adder in VLSI applications. Buffers are added to the test bench's input and output to create a more realistic setting [18, 25]. Buffers are used on both the inputs and outputs of an adder cell to cancel out the effect of input capacitance and maintain a constant loading condition. Several test bench configurations are used to simulate the proposed complete adder.

The standard configuration of these test beds includes three input buffers and two output buffers (Fig. 3). The sole distinction between these two simulation setups was the amount of adder cells employed between the input and output. The number of levels often began at two and increased from there. After the third stage (described in detail in Section IV-B), the carry propagation delay from the input to the output was seen to increase dramatically, on the order of a factor of two. For this reason, a three-stage simulation test bench has been chosen.In addition, this test bed might be used to monitor the performance characteristics (power and delay) of a second adder cell. This provided a real-time simulation setting for the cascaded technique, as the tested adder cell could use the output and input capacitances of neighbouring adder cells. The worst-case simulation results of the second full adder cell were taken into consideration for analysis and comparison, and numerous random signal patterns were applied at the inputs. For both 180- and 90-nm technologies, the suggested full adder's performance was analysed by changing the supply voltage.

4.4. PERFORMANCE ANALYSIS OF THE PROPOSED FULL ADDER

Both 90-nm and 180-nm technology simulations were performed on the suggested full, and the results were compared to those obtained from other possible adder designs reported in [1]–[11] and [15–24], with a focus on the hybrid design approach [1], [2], [19].

TRANSISTOR SIZES OF PROPOSED FULL ADDER

Transistor Name	180nm technology		90nm technology	
	Width (W) (nm)	Length (L) (nm)	Width (W) (nm)	Length (L) (nm)
Mn1, Mn6	400	180	120	90
Mp1, Mp6	800	180	240	90
Mn2, Mn3	400	180	120	90
Mp2, Mp3	800	180	360	90
Mn4, Mn5	400	180	120	90
Mp4, Mp5	400	180	120	90
Mn7, Mn8	400	180	360	90
Mp7, Mp8	400	180	600	90

The power-delay product (PDP), or energy consumption, has been minimised in the given example to optimise power and delay in the circuit. It was found that the transistors in the inverter circuits accounted for the majority of the design's power consumption, while the transistors in the transmission gates between Cin and Cout accounted for the majority of the design's carry propagation latency improvement. Table I provides the transistor sizes for the proposed full adder circuit in both the 90 nm and 180 nm technologies.

4.5. SCHEMATIC DIAGRAM OF THE PROPOSED FULL ADDER

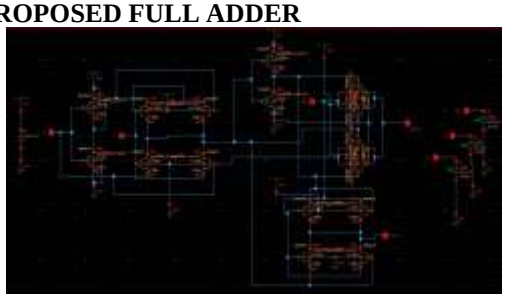

Fig.4.6. A Draught Circuit Diagram for a Full Adder

4.6. Timing diagram

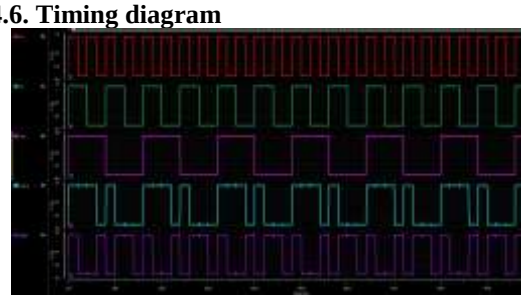

Fig.4.7. Schematic of the Proposed Full Adder's Timing

V. RESULTS AND DISCUSSIONS

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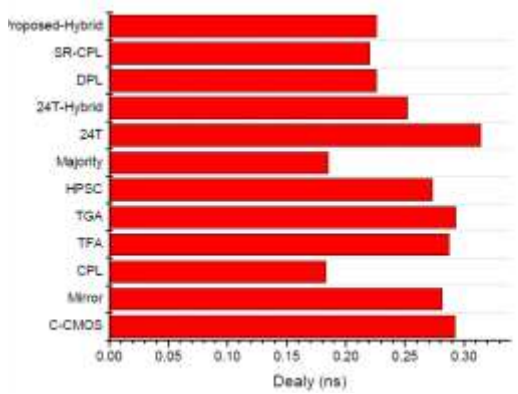

Fig. 5.1 THE 180-NITUDE TECHNOLOGY DELAY

We can see that the proposed hybrid system has a delay of 0.226 ns when compared to other systems built with 180 nm technology in the preceding graph.

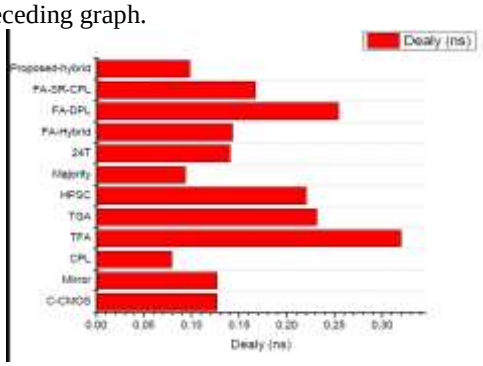

Fig. 5.2 SLOW PROGRESS ON 90 NM TECHNOLOGY

It can be seen from the above graph that the suggested hybrid system has a delay of 0.10ns, which is significantly lower than the delays of other systems built with 90 nm technology.

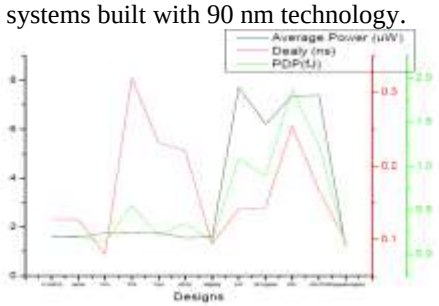

Fig. 5.3 90nm Technology Power Delay and PDP Averages

The preceding graph compares the proposed hybrid system to existing systems built with 90nm technology in terms of average power, latency, and PDP. Power consumption is 1.1965 uW, latency in nanoseconds is 0.098ns, and power delay product (PDP) is 0.117 f J for the suggested hybrid system. When put up against other current systems, it is seen to perform well.

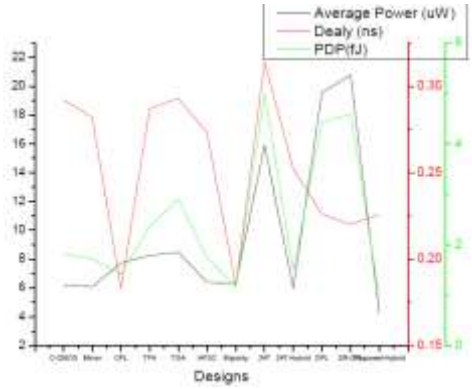

Fig. 5.4 180nm Technology Power Delay and PDP Averages

The preceding graph compares the proposed hybrid system to existing systems built with 180nm technology in terms of average power, latency, and PDP. The PDP (power delay product) for the proposed hybrid system is 0.956 f J, the delay ns is 0.226 ns, and power consumption is 4.232 uW. When put up against other current systems, it is seen to perform well.

PDP IN 180NM TECHNOLOGY

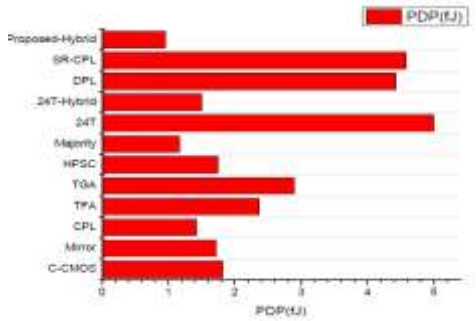

Fig. 5.5 Using 180nm Technology PDP

The accompanying diagram compares the PDP of the proposed hybrid system to that of existing systems built with 180nm technology. When compared to comparable systems, the proposed hybrid system has an extremely low PDP (0.956fJ).

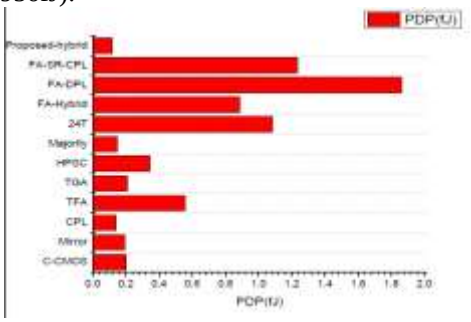

Fig. 5.6 Technology for PDP at 90 nm

For comparison, the PDP for existing systems built using 90nm technology and the proposed hybrid system is displayed above. When compared to comparable systems, the suggested hybrid system has an extremely low PDP (0.117fJ).

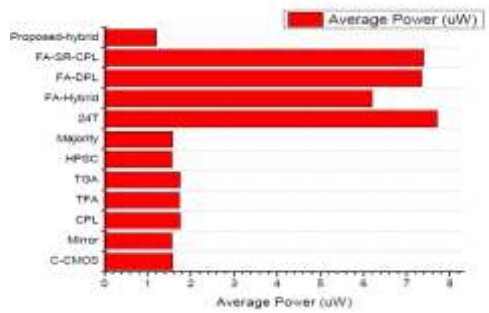

Fig. 5.7 Standard Power Consumption at 90 nm

The power consumption of the suggested hybrid system and competing systems based on 90nm technology is depicted above. When compared to other systems, the suggested hybrid system's power consumption is significantly lower (1.1965uW).

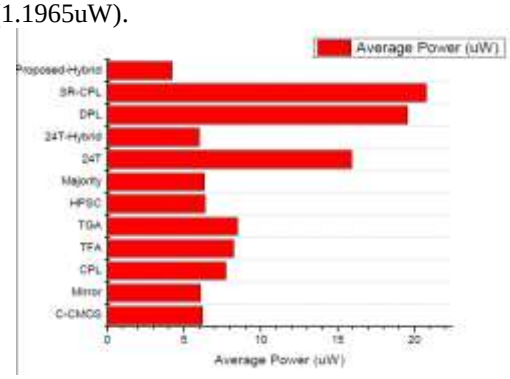

Fig. 5.8 Standard Power Consumption at 90 nm

Above, you can see a comparison between the energy consumption of the proposed hybrid system and that of other systems built with 180nm technology. When compared to previous systems, the power consumption of the proposed hybrid system is quite low, at only 4.232uW.

VI. CONCLUSION

- In this paper, we present the design of a hybrid 1 bit complete adder that combines CMOS and transmission gate logic.
- In this case, the XNOR module reduces power consumption by using a weak CMOS inverter.
- Signal propagation delays can be minimised by employing powerful transmission gates in the carry generating module.

FUTURE SCOPE

The proposed full adder can also be used to create a 32-bit carry propagation adder with buffers placed strategically throughout the addition process.

REFERENCES:

[1] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in *Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst.*, vol. 13 Apr. 2007, pp. 1–4.

[2] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[3] N. H. E. Weste, D. Harris, and A. Banerjee, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed. Delhi, India: Pearson Education, 2006.

[4] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Delhi, India: Pearson Education, 2003.

[5] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEE Proc.-Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.

[6] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[7] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[8] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[9] M. L. Aranda, R. Báez, and O. G. Diaz, "Hybrid adders for high-speed arithmetic circuits: A comparison," in *Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE)*, Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.

[10] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in *Proc. IEEE Workshop Signal Process. Syst. (SiPS)*, Taipei, Taiwan, Oct. 1999, pp. 713–722.

[11] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. Int. Symp. Circuits Syst.*, May 2003, pp. 317–320.

[12] S. Wairya, G. Singh, R. K. Nagaria, and S. Tiwari, "Design analysis of XOR (4T) based low voltage CMOS full adder circuit," in *Proc. IEEE Nirma Univ. Int. Conf. Eng. (NUiCONE)*, Dec. 2011, pp. 1–7.

[13] S. Goel, M. Elgamel, and M. A. Bayoumi, "Novel design methodology for high-performance XOR-XNOR circuit design," in *Proc. 16th Symp. Integr. Circuits Syst. Design (SBCCI)*, Sep. 2003, pp. 71–76.

[14] J.-M. Wang, S.-C. Fang, and W.-S. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," *IEEE J. Solid-State Circuits*, vol. 29, no. 7, pp. 780–786, Jul. 1994.

[15] P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," in *Proc. World Congr. Inf. Commun. Technol. (WICT)*, Dec. 2011, pp. 240–244.

[16] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design

of new full adder cell using hybrid-CMOS logic style," in *Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2011, pp. 451–454.
[17] I. Hassoune, D. Flandre, I. O'Connor, and J. Legat, "ULPFA: A new efficient design of a power-aware full adder," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.
[18] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *VLSI J. Integr.*, vol. 42, no. 4, pp. 457–467, Sep. 2009.
[19] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 718–721, Apr. 2011.
[20] J. L. Wyatt, Jr., "Signal propagation delay in RC models for interconnect," in *Circuit Analysis, Simulation and Design, Part II, VLSI Circuit Analysis and Simulation*, vol. 3, A. Ruehli, Ed. Amsterdam, The Netherlands: North Holland, 1987, ch. 11.
[21] M. Alioto, G. Di Cataldo, and G. Palumbo, "Mixed full adder topologies for high-performance low-power arithmetic circuits," *Microelectron. J.*, vol. 38, no. 1, pp. 130–139, Jan. 2007.
[22] X. Wu and F. Prosser, "Design of ternary CMOS circuits based on transmission function theory," *Int. J. Electron.*, vol. 65, no. 5, pp. 891–905, 1988.
[23] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power full adders based on majority-not gates," *Microelectron. J.*, vol. 40, no. 1, pp. 126–130, Jan. 2009.
[24] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 1, pp. 25–30, Jan. 2002.
[25] K. Navi *et al.*, "A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter," *Microelectron. J.*, vol. 40, no. 10, pp. 1441–1448, Oct. 2009.