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CODE STRUCTURE AND DECODING COMPLEXITY FOR DOUBLE AND TRIPPLE-ADJACENT ERROR CORRECTING PARALLEL DECODER

[1*]Dr.KallemNiranjanReddy

[1] Associate Professor & HoD, ECE Department, CMR Institute of Technology, Hyderabad, Medchal, Telangana

[1]nianreddy@gmail.com

ABSTRACT

Memories that operate in harsh environments, like for example space, suffer a significant number of errors. The error correction codes (ECCs) are routinely used to ensure that those errors do not cause data corruption. However, ECCs introduce overheads both in terms of memory bits and decoding time that limit speed. In particular, this is an issue for applications that require strong error correction capabilities. A number of recent works have proposed advanced ECCs, such as orthogonal Latin squares or difference set codes that can be decoded with relatively low delay. The price paid for the low decoding time is that in most cases, the codes are not optimal in terms of memory overhead and require more parity check bits. On the other hand, codes like the (24,12) Golay code that minimize the number of parity check bits have a more complex decoding. A compromise solution has been recently explored for Bose–Chaudhuri–Hocquenghem codes. The idea is to implement a fast parallel decoder to correct the most common error patterns (single and double adjacent) and use a slower serial decoder for the rest of the patterns. In this brief, it is shown that the same scheme can be efficiently implemented for the (24,12) Golay code. In this case, the properties of the Golay code can be exploited to implement a parallel decoder that corrects single- and double-adjacent errors that is faster and simpler than a single-error correction decoder. The evaluation results using a 65-nm library show significant reductions in area, power, and delay compared with the traditional decoder that can correct single and double-adjacent errors. In addition, the proposed decoder is also able to correct some triple-adjacent errors, thus covering the most common error patterns.

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I INTRODUCTION

With the rapid growth of digital communications, such as Digital Audio Broadcasting (DAB) and ATM systems, increased data rate and advanced error control coding techniques are required. Thus, the parallelism inherent in the decoding algorithm and the area-efficient high-speed VLSI architectures must be exploited. The (24,12,8) extended Golay code is a well-known error-correcting code, which has been successfully applied in several existing communication systems to improve the system bit-error-rate (BER) performance. One goal of this research was to provide a strong error protection for the important head information in the transmission of the high quality compressed music signal of the DAB system. The parallel Golay decoder can be, of course, used generally to protect the data transmission or storage against channel errors for high speed data processing. A number of soft-decision decoding of the (24,12) binary Golay code were intensively investigated in the last few years and detailed analysis of computational complexity were discussed. However, none of these algorithms have been realized efficiently with parallel VLSI circuits. This paper introduces a full parallel permutation decoding technique with look-ahead error-correction and a fast soft-decision decoding for (24, 12, 8) extended Golay code. The area-efficient parallel VLSI architectures and the computer simulation results are also presented. The look-up table used in this improved algorithm consists of syndrome patterns and corresponding error patterns which have one to three errors occurred in the message block of the codeword. Then the look-up table contains only 25 syndrome patterns and corresponding error patterns. Suppose that there are only three or less errors occurred in (15, 5 ,7) BCH codeword. Due to the latter part of H is a 10x10 identity matrix and S = eHT , if the weight of S w(S)≤3, it means at most three errors only occurred in the parity check block and the location of 1 in S is just the error location in the parity check block. Then shift the syndrome right 5 bits to form a 15-bit length word and minus (modulo 2) the received codeword to decode. If w(S) ≥ 4, it means at least one error occurred in the message block. First, the syndrome minus (modulo 2) all syndrome patterns in the table to obtain the difference and compute the weight of these difference, respectively

II RELATED WORKS

Enhanced Detection of Double and Triple Adjacent Errors in Hamming Codes Through Selective Bit Placement has been explained in[6].In this paper, a technique to increase the probability of detecting double and triple adjacent errors when hamming codes are used. The enhanced detection is achieved by placing the bits of the word such that adjacent errors result International Journal of Applied Engineering Research ISSN 0973-4562 Volume 11, Number 6 (2016) pp 4440-4444 © Research India Publications. http://www.ripublication.com 4441 in a syndrome does not match that of any single error. LowPower Compact Composite Field AES S-Box/Inv S-Box design in 65nm CMOS using Novel XOR Gate has been described in [1]. This paper presents a full custom CMOS design of S-Box/Inv S-Box with low power GF (28) Galois Field Inversions based on polynomial basis, using composite field arithmetic. The S-Box/Inv S-Box utilizes a novel low power 2-input XOR gate with only six devices to achieve a compact module implemented in 65 nm IBM CMOS technology. This design indicates a power dissipation of only around 0.09µW using a 0.8V supply voltage. Research and Implementation of SEC-DED Hamming Code Algorithm has been briefly explained in [5]. In this paper, the Hamming Code scheme is used to protected the external memory, due to the parity memory having 8 bits width, a(40,32) hamming code is used, it is on the base of (39,32) Hsiao code, adding a parity bit to minimize the probability of 3 bits faults corrected in error. Hamming SEC-DAED and Extended Hamming SEC-DED-TAED Codes through Selective shortening and Bit Placement has been described in [7]. In this paper, specific matrices for single-error-correction double adjacent error detection (SEC-DAED) hamming codes are presented. They will provide a code capable of correcting single errors and detecting double adjacent errors. Additionally, Single-Error-Correction Double-Error-Detection Triple Adjacent Error Detection (SEC-DED-TAED) codes are generated from an extended hamming code. Efficient Implementation of Hamming SEC-TAED Code Algorithm for Data Communication has been explained in [4]. In this paper, the design of Single Error Correction-Triple Adjacent Error Detection (SEC-TAED) codes through Bit Placement algorithm is presented with less number of parity bits. In the proposed method, the detection efficiency is increased when compared to conventional SEC-TAED. Design of a High Speed and Area Efficient Optimized Mixcolumn for AES has been designed in [3].In this paper,

a novel optimized Mix-Column is designed for AES decryption through VLSI design environment. The proposed MixColumn is incorporated into AES Decryption for improving the performance in terms of VLSI concerns (area, delay and power). Modified Hamming Codes with Double Adjacent Error Correction along with Enhanced Adjacent Error Detection has been explained in[2].In this paper, modified hamming codes to enhance adjacent error detection along with double adjacent error correction is presented. The modified hamming codes can correct single and double adjacent errors and can detect double errors and triple adjacent errors. On Forward Error Correction with Hamming Code for Multipath Communications have been explained in [8]. In this paper, the performance bound in the high error-rate networks and integrated multipath communication and Hamming code (11-7). Using the Markov model, the performance of Multipath Hamming Code based Forward Error Correction (MHCFEC) is analyzed and compared with Multi-Path Power Control (MPC). Bit-Level Soft-Decision Decoding of Double and Triple-Parity Reed-Solomon Codes Through Binary Hamming Code Constraints has been described in [9] .This paper discussed bit-level soft-decision decoding of double and triple-parity Reed-Solomon (RS) codes through binary Hamming Code constraints. Based on the binary image of RS code, they first present the new expressions of the associated parity-check equations. These expressions indicate that each parity-check equation of RS code with roots α i ($0 < i < 3$) over GF(2q) can be viewed as parity-check equations of a compound Hamming code over GF(2)

III PROPOSED SCHEME

The concept would be to implement a quick parallel decoder to fix the most typical error patterns (double and single adjacent) and employ a slower serial decoder throughout the patterns. The extended code includes a minimum distance of eight, and for that reason can correct 3-bit errors Vanjari Soumya Latha * et al. (IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH Volume No.5, Issue No.4, June – July 2017, 6839-6840. 2320 –5547 @ 2013-2017 http://www.ijitr.com All rights Reserved. Page | 6840 and identify 4-bit errors. It's been utilized in many applications including space missions that need strong error correction abilities. Within this brief, a double and single-adjacent error correcting parallel

decoder for that (24,12) extended Golay code continues to be suggested [1]. The decoder uses the qualities from the code to attain a competent. The decoding from the Golay code is performed in a number of steps and needs several clock cycles. Just one-error correcting parallel decoder could be implemented by computing the syndrome and evaluating in parallel using the 12 data bit and also the 12 check bit posts. When there's a match that bit is remedied. To judge the advantages of the brand new decoder, it's been implemented in Highdensity lipoprotein and mapped to some 65-nm library. As MCUs affect cells which are close together, numerous codes that may correct doubleadjacent or triple-adjacent errors happen to be lately suggested. These codes, oftentimes, don't require additional parity check bits as well as in the remainder require just one or two additional bits [2]. A 4-bit error might not be even detected through the SEC-DAEC decoder. Therefore, the entire syndrome can be used for comparisons out of all cases to make sure that triple errors don't trigger miscorrections and 4-bit errors are detected. The suggested parallel decoder also offers to identify errors it cannot correct. In individual's cases, the serial decoder can be used to fix the mistake. The logic required to identify individual's errors is only a look into the no zero syndrome along with a make sure that no comparators has detected a match. Part one could be implemented having a 12- input OR gate and also the second with another 24- input OR gate. Finally, the ability consumption is considerably smaller sized compared to the standard SEC-DAEC decoder and other alike to that particular from the SEC decoder.

IV RESULTS:

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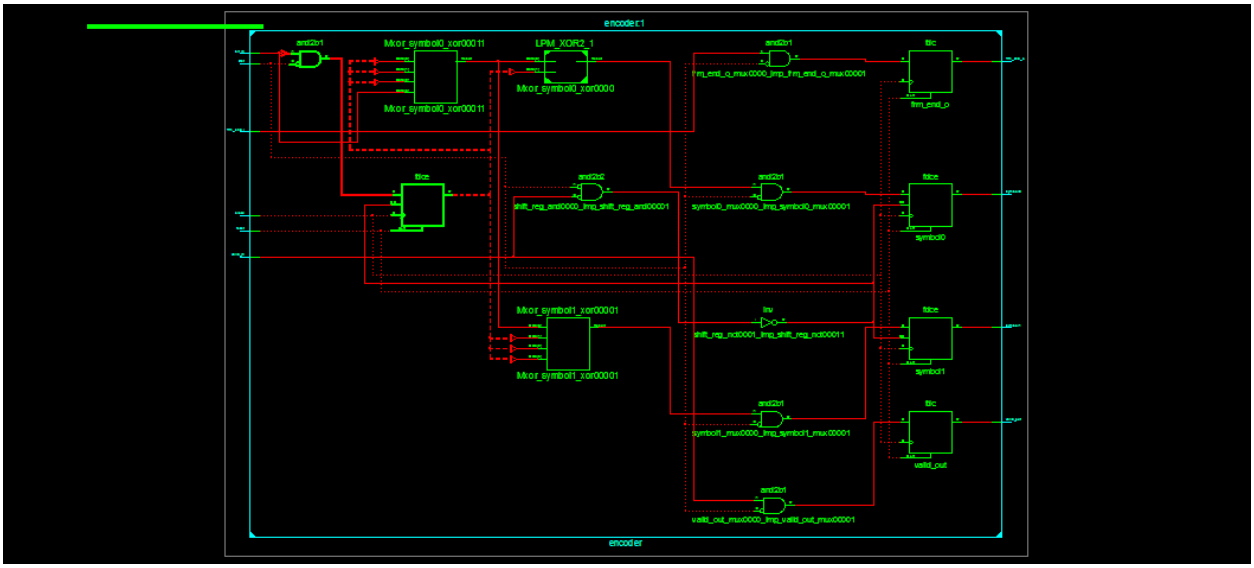

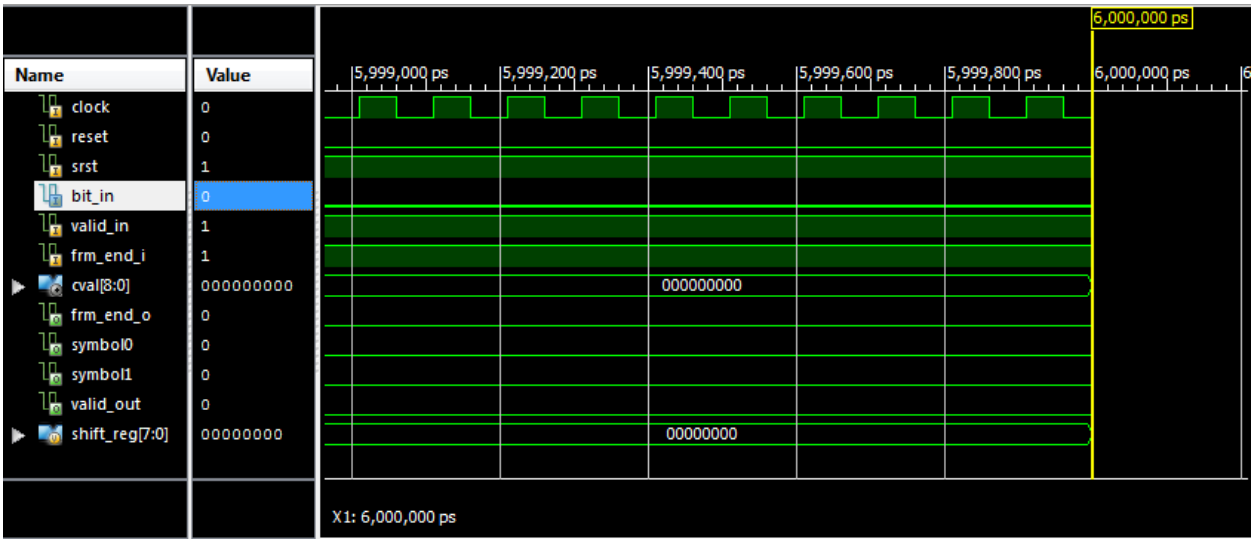

V. CONCLUSION

The suggested parallel SEC-DAEC decoder continues to be implemented in High-density lipoprotein and mapped to some TSMC 65-nm technology library using Synopsys Design Compiler. The standard SEC and SEC-DAEC decoders are also carried out to show the advantages of the brand new decoder. The cost compensated for that low decoding time is the fact that generally, the codes aren't optimal when it comes to memory overhead and wish more parity check bits. However, codes such as the (24,12) Golay code that minimize the amount of

parity check bits possess a more complicated decoding. ECCs adds parity check bits to every memory word to identify and proper errors. This involves an encoder to compute individual's bits when contacting the memory along with a decoder to identify and proper errors when studying in the memory. These components boost the memory area and also the power consumption, and may also lessen the access speed. The suggested parallel decoder as discussed before has the goal of correcting double and single-adjacent bit errors. The initial step would be to put the bits within the memory so that data and parity bits are interleaved. One solution to make sure that the MCU errors could be remedied would be to interleave the items of different logical words to ensure that an MCU affects one bit per word. This is dependent on the observation the cells impacted by an MCU are physically close. Interleaving, however, includes a cost because it complicates the memory design.

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