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Design And Implementation Of Low Power-High Performance Mixed Logic Line Decoders

[1]A VEERESH 21tq1a0405@siddhartha.co.in [1] S ANUSHA 21tq1a0408@siddhartha.co.in [1]P RANI 22tq5a0406@siddhartha.co.in [2]Dr. M Krishna Chaitanya krishnachaitanya.ece@siddhartha.co.in

SIDDHARTHA INSTITUTE OF TECHNOLOGY & SCIENCES Korremula Road, Ghatkesar, Medchal-Malkajgiri (Dist)-500 088

ABSTRACT

This study looks at Modified Mixed Logic Design (MMLD), which combines three distinct logic techniques: Gate Diffusion Input (GDI) technology, By contrasting two decoder systems—one with 14 transistors and the other with 15—the objective is to lower power consumption and delay time. In each scenario, both standard and inverted decoders are used. The paper claims that the suggested decoders provide complete voltage swing with a much lower transistor count (around 12 transistors) than traditional CMOS logic, which leads to lower power consumption and faster delay times. Using SPICE simulations, the performance of the suggested 12-transistor 2x4 decoder at the 16nm technology node has been assessed, and the findings are better than those of conventional logic systems.

I.INTRODUCTION

Integrated circuit logic gates often make use of static complementary metal-oxide semiconductor (CMOS) circuits. Integrating semiconductors, CMOS (Complementary Metal-Oxide-Semiconductor) circuits use pMOS and nMOS pull-down networks. These circuits will not let you down when it comes to important performance measures such as noise and device fluctuation resistance. Amazing CMOS circuit features abound, including small transistor sizes and reliable low-voltage performance. In contrast, CMOS circuits are severely limited in that they can only take inputs at the transistors' gate terminals. Because of this, cell-based logic has emerged, which limits the adaptability of designs. Faster, more power-efficient, and smaller than complementary metal-oxide-semiconductor (CMOS) logic, which came out in the '90s, is Pass Transistor Logic (PTL). The inputs of pass transistors may be connected to both the gate and the source/drain diffusion terminals when building circuits. Permit me to explain the fundamental difference. Either pMOS or nMOS transistors alone may form a pass transistor circuit, or you can link them in parallel to form a transmission gate. The need for tiny, quick, and power-hungry logic circuits is on the rise due to the ever-increasing development of VLSI (Very Large Scale Integration) technologies, such as voltage scaling and shrinking. For high performance

computers, it is crucial to design systems that use as little power as possible. This includes digital signal processors and microprocessors.

II.LITERATURE SURVEY

Because of its effectiveness, resistance to noise, and device variation tolerance, static CMOS logic is often used to build the logic gates of integrated circuits. Because it is built from complementary nMOS pull-down and pMOS pull-up networks, the CMOS circuit's reliable performance is not affected by the voltage or size of the transistor. The key advantage of complementary metal-oxide semiconductors (CMOS) is its scalability, which enables low-voltage operation with little design complexity. Design flexibility is diminished and cell-based synthesis becomes more challenging in static CMOS due to inputs being applied solely to the transistor gates.

When compared to traditional complementary metal-oxide-semiconductor (CMOS) logic, pass-transistor logic (PTL) has many benefits, including faster processing times, less space requirements, and lower power consumption. PTL was developed in the 1990s to replace CMOS. One notable difference between PTL circuits and CMOS circuits is the ability to apply inputs to the gate, source, and drain terminals of transistors in PTL circuits. You can build pass-transistor circuits using individual nMOS or pMOS transistors, or you can use a mix of the two types to create a transmission gate. Because of its adaptability, PTL is a great material for making compact yet robust circuits.

III.EXISTING METHOD

The word-line is driven by synchronization circuits on each select-line; these circuits often include a buffer, sometimes known as a word driver. A content-addressable memory's match lines may be precharged using an AND-NOR decoder architecture that is very similar to the fundamental selective precharge approach described in [6]. A simulated NOR decoder is shown in Figure 1. In memory, the variables stand for the amount of address bits and rows, respectively. 4.10 Mixed-Logic Lines 2-4 and 4-16 Low-Power, High-Performance Decoder Design Transmission gates, the fundamental switch element of multiplexers, are widely used in combinational logic circuits that rely on XOR operations, such as complete adders. Still, we think about how to include them into AND/OR logic, which has proven effective in line decoders. In

Figures, we can see the two-input TGL AND/OR gates. Even if they don't restore for all input combinations, they are entirely swinging. There are two primary types of pass-transistor logic circuits: those that use nMOS pass transistors exclusively, such as CPL, and those that combine nMOS and pMOS pass transistors, such as DPL and DVL. Here we have a look at the DVL style, which is an upgrade above DPL and needs less transistors to keep full swing operational. In Figures, you can see the DVL AND/OR gates with two inputs. Similarly to TGL gates, they are nonrestoring and full-swinging. The number of transistors required by TGL/DVL gates is reduced from four for CMOS NAND/NOR gates to three, provided that complementary inputs are accessible. There may be a reduction in transistor use when employing TGL/DVL gates in decoders, which have high fan out circuits with few inverters that may be utilized by several gates. The asymmetry, or imbalance, of the input loads is a defining feature of these gates. Figure 2 shows that we labeled the two inputs to the gate as X and Y, respectively. When using a TGL gate, input X controls the three transistors' gate terminals and input Y goes to the output node via the transmission gate. Two transistor gate terminals are regulated by input X in DVL gates, whereas one terminal is regulated by input Y, which flows via a pass transistor to the output. A gate's X input represents its control signal, whereas its Y input represents its propagation signal. Because of this imbalance, signal arrangement may be carried out, meaning that which input is used as a control signal and which as a propagation signal in every gate.

IV.PROPOSED METHOD

The 2-4LP, 2-4LPI, 2-4HP, and 2-4HPI topologies for 2-4 line decoders were all developed using this method. With respect to transistor count and power-delay performance, these topologies outperform conventional CMOS decoders. Also included were four new topologies for 4-16 line decoders: 4-16LP, 4-16LPI, 4-16HP, and 4-16HPI. The integration of predecoding circuits based on mixed-logic 2-4 decoders and post decoders constructed into static CMOS allowed for the development of these, which are now used in many applications. Several comparison spice simulations were run at 32 nm, and the findings usually backed the obvious benefits of the proposed designs. For applications that value space and power efficiency, the 2-4LP and 4-16LPI topologies are ideal. All three of the 4-16 topologies—4-16LP, 4-16HPI, and 4-16HP—as well as the 2-4LPI, 2-4HP, and 2-4HPI designs—were generally effective and practical. Therefore, they may serve as foundational elements for the construction of more complex combinational circuits,

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such as multiplexers, decoders, and others, each with its own unique set of performance demands. The low power characteristics and reduced transistor count may also be useful for SOI devices as well as bulk CMOS devices. Because they need to be implemented at the layout level, the produced circuits are suitable for RTL design and standard cell libraries.

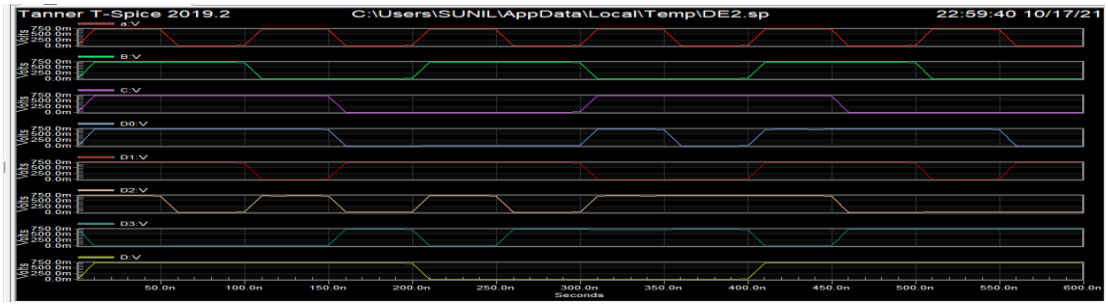

Figure 5.2: Line decoder simulation results based on 2-4 LPI

A line decoder based on 2-4 LPI is presented in the above picture as a simulated result. Downside of the 14 transistor low power decoder topologies that were previously mentioned is the worst-case delay that comes from the complementary propagation signal that is employed in minterms D0 and I3. You may circumvent this restriction by building these minterms using regular CMOS logic gates; they don't need complementary inputs. While a CMOS NAND gate is used to construct I3, a CMOS NOR gate is used to create Minterm D0. There is an extra transistor in every topology. The resulting decoder architecture, called High Performance (HP) topology, enhances power and delay performance by integrating three types of logic (CMOS, TGL, and DVL) into a single circuit. You can see the 2-4 HP and 2-4 HPI decoder schematics in the figure that it is attached to.

Line decoder schematic based on 2-4 HPI

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Vol 12, Issue 4, 2024

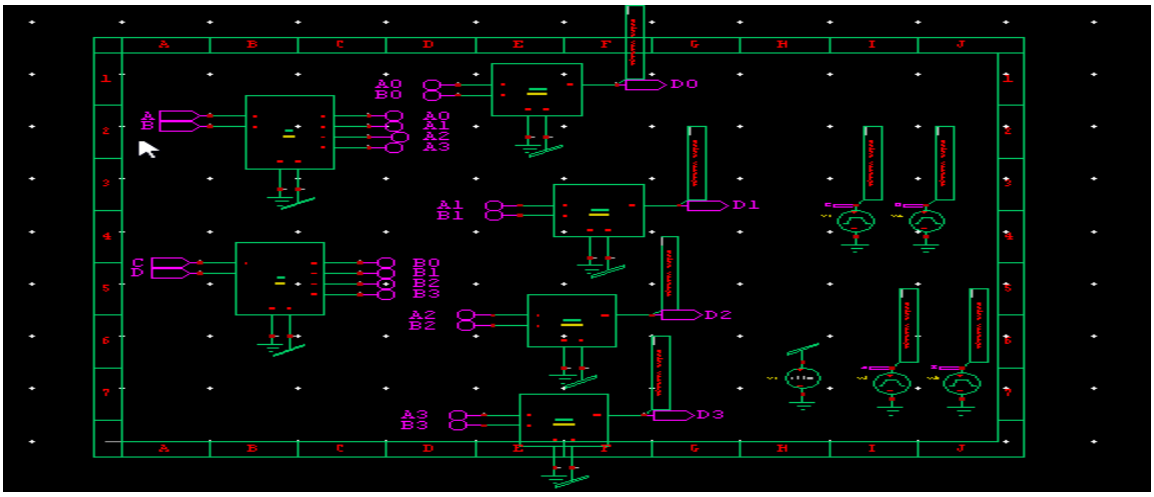
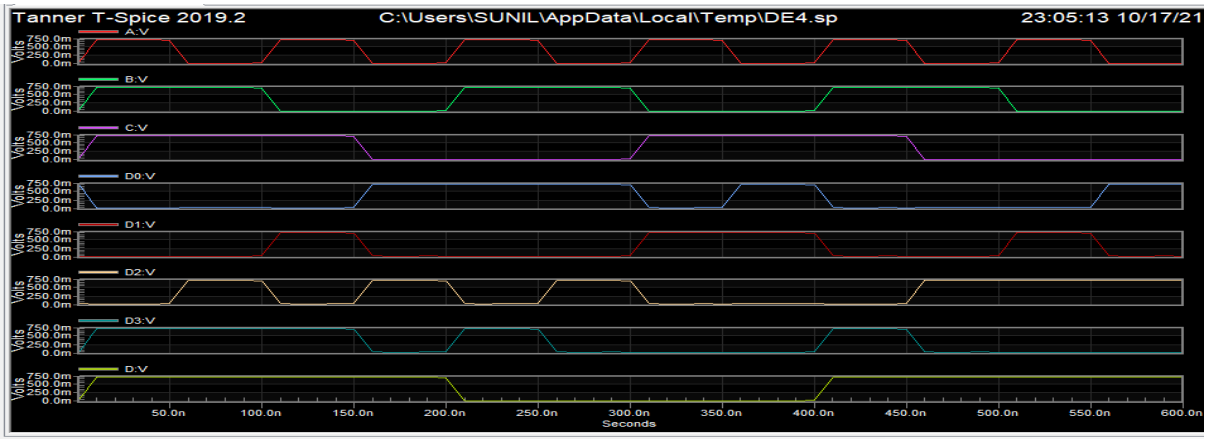


Figure HPI decoder schematic

One drawback of the low-power topologies mentioned earlier in relation to worst-case delay is that in the situations of D0 and I3, the propagate signal is complementary A. Still, static CMOS gates can get the job done for D0 and I3 even when complementary signals aren't available. Specifically, by replacing D0 with a CMOS NOR gate and I3 with a CMOS NAND gate, each topology may have one transistor added to it. A considerable decrease in latency is provided by the new 15T designs with just a little increase in power consumption. They go by the acronyms "2-4HP" (9 nMOS, 6 pMOS) and "2-4HPI" (6 nMOS, 9 pMOS), with "HP" standing for "high performance" and "I" for "inverting." Figure shows the 2-4 HP and 2-4 HPI schematics.



displays the simulation results for 2-4 HPI decoders.

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Above you can see the 2-4 HPI line decoder simulation results. On a micro level, CMOS logic circuits may not be as efficient as pass transistor logic circuits due to the latter's higher transistor count. One problem with pass transistor circuits is that they don't fix anything, as mentioned above. Consequently, adding more and more layers of these logic circuits causes them to degrade quickly. By combining the alternating phases of non-restoring and restoring logic circuits, one may overcome this mixed logic design architecture. To get the best possible outcomes, this hybrid logic topology makes use of the best features of both logic approaches.

V.CONCLUSION

This project has been verified using Mentor Graphics' 16nm technology. An effective mixed logic decoder architecture has been created by combining static CMOS, TGL, and DVL circuits. We propose two novel topologies for the development of low power, high performance decoders. Every single one of these cases makes use of either a conventional or an inverted 2-4 or 4-16 decoder, with or without enable input. The 2-4 and 4-16 LP LPI decoders are suitable for uses where space and power dissipation are major design concerns, according to the simulation results. Using fewer transistors, they increase power while introducing a delay penalty. Using fewer transistors while improving power and delay performance, the 2-4 and 4-16 HP, HPI decoders outperform traditional CMOS logic decoders in almost all cases. This leads to reduced power consumption, quicker operation, and fewer transistors used by the proposed mixed logic decoders. Power consumption for the recommended 12 Transistors 2X4 Decoder is 2.95 Mw. A total decrease of 30% in power consumption has been achieved by using the proposed method.

VI. FUTURE SCOPE

The suggested mixed-logic decoders are ideal for contemporary VLSI applications as they use less power, run faster, and have fewer transistors. With a power dissipation of just 2.95 µW, the 12-transistor 2x4 decoder architecture reduces power usage by 30% when compared to traditional systems. Future studies will examine whether these decoders can be scaled to sub-5nm technology nodes, optimize them for sophisticated memory systems, increase their resilience to process fluctuations, incorporate them into high-speed computing systems, and use machine learning to further optimize them. These developments may result in even more effective, high-

performing decoders for a range of next-generation applications, including ultra-low-power memory systems and artificial intelligence computers.

REFERENCES

1. Roy, K., & Prasad, S. C. (2000). Low-Power CMOS Digital Design. Wiley-Interscience.
2. Zhao, Y., Wu, H., & Irwin, M. J. (2017). High-Performance Memory Testing and Design for the Internet of Things. Springer.
3. Rajasekaran, K. S., & Iyengar, S. S. (2003). Design of Low-Power VLSI Circuits. Springer.
4. Ghaffarian, R., Rabaey, J. M., & Pati, D. S. (2017). 16 nm CMOS Technology for Low-Power Applications. Springer.
5. Kang, S. M., & Leblebici, Y. (2003). CMOS Digital Integrated Circuits: Analysis and Design (3rd ed.). McGraw-Hill.
6. Mohan, M., & Kato, T. (2012). A Review of Low Power Techniques for VLSI Systems: Hybrid Decoders and Their Applications. Journal of VLSI Design & Technology, 40(3), 45-60.
7. Agarwal, A., & Soni, P. (2015). Power and Area Efficient Hybrid Decoding Techniques for Memory Design. International Conference on VLSI Design, 1-6.
8. Hamoui, M. A. (2009). Low-Power Digital VLSI Design for Memory Devices. Springer.
9. Amin, S., & Fatima, M. (2016). Design of Area and Power Efficient Memory Decoders Using 16 nm FinFET Technology. IEEE Transactions on VLSI Systems, 24(6), 2051-2062.
10. Raghavan, K. V. (2013). Low-Power and Area-Efficient Memory Architectures for Embedded Systems. Journal of Low Power Electronics, 9(4), 400-411.
11. Burt, D. A., & Karmakar, N. (2019). Low-Power and High-Speed Hybrid Decoders in Nanometer CMOS Technology. IEEE Transactions on VLSI Systems, 27(9), 1823-1834.