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COMPARATIVE ANALYSIS 4:1 MULTIPLEXER USING CMOS TECHNOLOGY NANOMETER REGIME

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ABSTRACT

Miniaturisation has made power consumption and die area reduction the two most important criteria for each new circuit design. An important digital circuit is the multiplexer. Among the many possible circuit implementations are adders, subtracters, and form SOP functions. This study analyses several technological nodes using the multiplexer's power and latency metrics. And, OR, and NAND gates with TG gate types have been created using regular MOSFETs in 32 nm and 45 nm technologies. Here we compared the following performance metrics: average power, power delay product, energy-delay product, delay as a function of process parameters, and supply voltage and temperature. A lower-tech node consumes more power than a higher-tech one, but it takes up more space. But high-speed is the most basic kind of technology.At 32 nm, the supply voltage drops by 33%, the delay increases by 20.94%, and the power drops by 90.82%; at the same wavelength, the delay increases by 193.72% and the power drops by 84.75%.

Keywords: *MOSFET, Adders, Subtracters, Multiplexer and Transmission Gate(TG)*

INTRODUCTION

A basic digital circuit known as an A4:1multiplexer (MUX) may take four input signals and combine them into a single signal that can be delivered to an output line. Given its scalability, low power consumption, and exceptional noise immunity, CMOS (Complementary Metal-Oxide-Semiconductor) technology is relied upon by modern digital designs, especially in the nanometre domain (such as 28nm and 14nm technologies).In order to build a 4:1 multiplexer in the nanometre range using CMOS technology, this work investigates several design techniques.

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There are a number of advantages to using CMOS technology with n-type and p-type MOSFETs to do logic functions.The low static power consumption is a major advantage of CMOS circuits as they only take power when the signal strength changes. Electrical noise is less of an issue with CMOS circuits because of their large noise margins. Crucial in the ever-changing semiconductor manufacturing environment is the scalability of CMOS technology, which enables performance to increase with lower feature sizes.The layout of a 4:1 multiplexer may take several forms. The most common kind of multiplexer utilised is the transmission gate, which is effectively a hybrid of the NMOS and PMOS transistors.To enable the chosen input to reach the output, control signals in this system activate the appropriate transmission gate. This method is quick and doesn't utilise much static electricity, but it may be difficult to set up and requires more room. Combining AND, OR, and NOT gates is another typical approach in logic gate design that achieves the required selection logic. The inputs are processed and the output is produced by this design using selection signals. Due to static power losses, this approach often consumes more power than gearbox gate systems, despite its simplicity and endurance. The pass transistor logic method relies on these selectlines to send logic values via NMOS transistors. There is less need for transistors in this design, making it more space-efficient. Avoiding voltage deterioration and ensuring signal integrity requires meticulous planning, especially when using NMOS transistors. We use a variety of performance indicators to assess these designs. When compared to logic gate implementations, which often have larger delays owing to the larger number of gates involved, transmission gate designs frequently have the shortest delays because of their efficiency. There is no critical component related to the propagation delay. Pass transistor logic may operate in the middle ground, depending on the levels of transmitted voltages. The most energy-efficient gate design is a gearbox gate due to its small dynamic power requirement and low static consumption. While logic gate implementation often consumes more power overall and pass transistor logic achieves a decent balance in terms of static consumption, it might have problems with charge sharing. Efficiency in terms of space is also very important. Area

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requirements may be much higher than those of transmission gate designs due to the use of complementary transistors in logic gate implementations. The most space-efficient solution is frequently pass transistor logic, but its application requires careful consideration. The methods differ with respect to the integrity of the signals. Because of the complimentary actions of the transistors, transmission gate designs provide strong signal integrity, in contrast to logic gate implementations that give enough integrity but are susceptible to noise margins.Although pass transistor logic is space-saving, additional buffering may be required to prevent signal degradation. When choosing a design for a 4:1 multiplier employing CMOS technology, it is important to balance certain performance factors based on the needs of the nanometre domain application. In contrast to logic gate implementations, which provide simplicity and durability but increase power consumption, transmission gate designs are known for their speed and power efficiency. Properly limiting voltage degradation throughout the design process is crucial, even when using pass transistor logic may enhance area efficiency. In the end, the particular limitations of the application should dictate how factors like power, speed, area, and signal integrity are considered.

Literature Survey

An Overview of Literature Survey

Crucial research areas include the design and optimisation of multiplexers, especially 4:1 multiplexers, within the context of CMOS technology in the nanometre regime.Focussing on performance measurements, design techniques, and scaling implications, this literature review examines several research that address the difficulties and developments in this area.

First, complementary metal-oxide semiconductors (CMOS) and nanometre scaling have been the foundation of digital circuit design for a long time because of their low power consumption and large noise margins. But problems like short-channel effects and higher leakage currents become major concerns when transistors shrink down to the nanometre region. In his discussion of the critical issues with nanoscale technology, Borkar (2016) stresses the importance of creative design approaches to preserve circuit performance. The behaviour of complementary metal-oxide semiconductor (CMOS) devices is

complicated as their dimensions reduce, as discussed in detail by Wang et al. (2012), who also note that a better grasp of device physics at lower sizes is required.

Multiplexer Design Methods

Multiplexers built using complementary metal-oxide semiconductor technology (CMOS) often have both static and dynamic configurations. Static multiplexers are often simple and reliable since they use a basic configuration of transistors. Dynamic multiplexers, on the other hand, are capable of faster speeds but add complexity to charge storage and scheduling. In their detailed analysis of the pros and cons of using dynamic vs static logic in multiplexer design, Shafique et al. (2015) provide a thorough examination of the topic. Their research shows that static designs tend to be more stable and predictable in many environments, even when dynamic designs might be quicker.

Performance metric analysis in Propagation delay, power consumption, and area efficiency are three important performance criteria for multiplexers in the Nanometre Regime. Parasitic capacitance, which becomes more important as devices scale, influences propagation latency, as Chenetal. (2018) explains. According to their research, in order to achieve optimal performance, design techniques should take these parasitic effects into consideration. Focussing on the large influence of leakage currents in sub-45 nm technology, Zhang et al. (2020) further elucidate on power usage. The significance of controlling static power dissipation, which may become a determining element in the overall performance of a circuit, is highlighted by their examination of power optimisation strategies.

Analyses of Multiple UX Designs

We can learn a lot about the performance trade-offs by comparing various multiplexer architectures. A research comparing static and dynamic 4:1 multiplexers across different technological nodes was carried out by Kumar et al. (2019). The study emphasised the trade-offs between speed and power efficiency. While dynamic designs might improve speed, their findings imply that they could reduce power efficiency, which is a major concern in low-power applications. The results are in agreement with those of Taneja and Prakash (2021), who provided a framework for comprehending the impact of design decisions on circuit performance by analysing propagation delay variations in multiplexers using various CMOS technologies.

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5. New Progress and What's Next

To get around the problems with conventional planar CMOS designs, new studies have looked at other technologies like Fin FETs. Improved electrostatic control and decreased short-channel effects are two benefits of Fin FET technology that Lee et al. (2021) point out, making it a viable option for future multiplexer designs. Gao et al. (2020) focusses on low-power designs in 4:1 multiplexers employing Fin FET technology, which shows a trend towards adopting sophisticated manufacturing processes to improve nanoscale performance.

The design of 4:1 multipliers employing CMOS technology in the nanometre range has seen both significant advances and persistent problems, as this literature review demonstrates. The significance of taking design techniques, performance measures, and developing technologies into account while aiming for optimum circuit performance is emphasised by the synthesis of ideas from different research. The results provide the groundwork for the project's future multiplexer design comparison, which hopes to aid in the creation of high-performance digital circuits that are both efficient and effective.

3. Existing System

IntroductionofGateLevelDesignof4X1MUX

A multiplexer may combine various data sources into one output depending on the inputs chosen by the controller. For every 2n input lines, there must be n selection lines, or for every N input lines, there must be log2(N) lines. Aside from multiplexers, other names for them include "N-to-1 selectors," many-to-one circuits, universal logic circuits, and parallel-to-serial converters. Their main job is to make the most efficient use of the time and capacity available in a network in order to transport data as quickly as possible.

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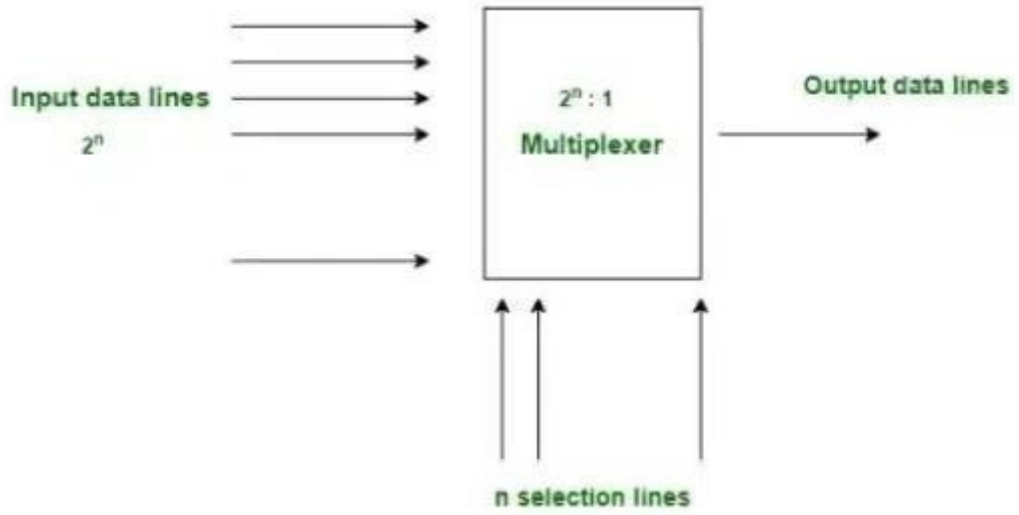

Fig3.1: Multiplexer

Existing Method: The four inputs of a 4×1 multiplexer are I0, I1, I2, and I3, whereas the single output, Y, is determined by the selection lines S0 and S1. The selection lines' binary values dictate the multiplexer's output.

- WhenS1S0=00,theinput I0isselected.
- WhenS1S0=01,theinput I1isselected.
- WhenS1S0=10,theinput I2isselected.
- WhenS1S0=11,theinput I3isselected.

TruthTableof4×1Multiplexerisgivenbelow.

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Table1:4x1Multiplexer

Circuit Diagram of 4×1 Multiplexers

Using truth table the circuit diagram can be given as

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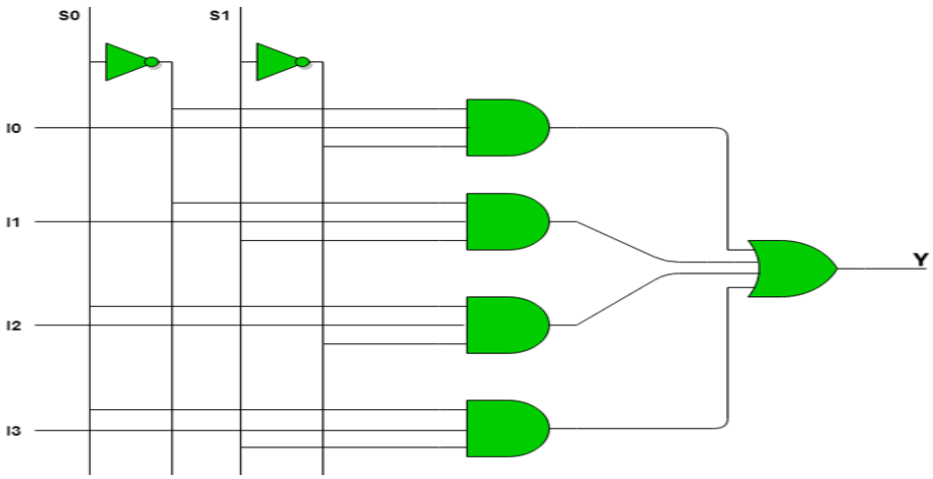

Fig3.2:Circuit Diagram of 4×1 Multiplexers

One use for multiplexers is as a general-purpose combinational circuit. Multiplexers may be used to build any of the common logic gates.

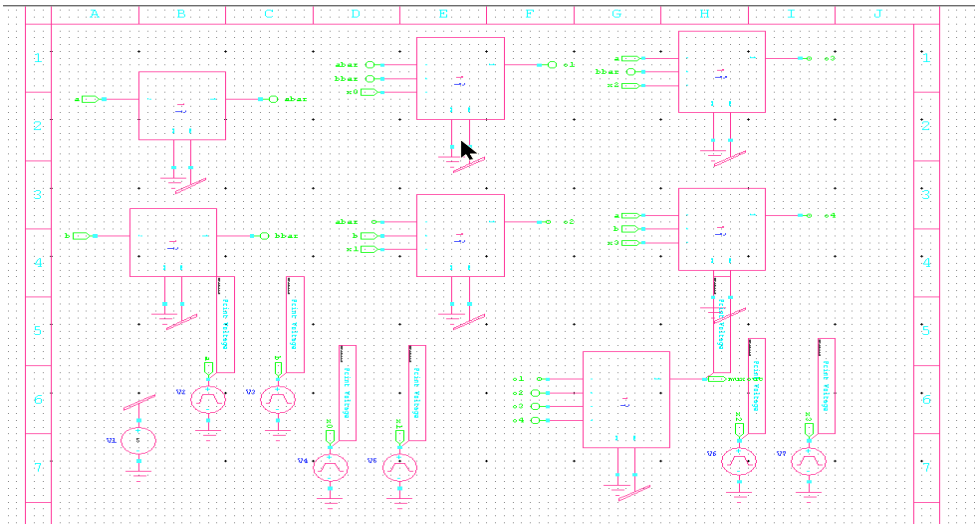

Fig3.3: 4*1 MUXUsing250nmTechnology

PowerAnalysisof4×1Multiplexersusing250 nm

The simulation shows a noticeable fluctuation in power usage, according to the power analysis of the 4×1 multiplexer in a 250nm CMOS process. Over the specified time period (from 0 to 5e-07 seconds), a low degree of energy utilisation was indicated by an average power usage of 658.83 µW. On the other hand, the power consumption peaks at

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1.01853e-07 seconds, which is more than 14.58 mWata specific time.Transient switching activity, a typical cause of dynamic power consumption in CMOS circuits, is probably to blame for this excessive peak power. Whenever the input statuses of the multiplexers change or the internal capacitive nodes of the multiplexers charge or discharge, this phenomenon occurs. Also, the simulation starts with a minimum power of 6.41 nW at time 0, so it's conceivable the circuit is in a low-power idle state before anything major happens. This process node experiences no power loss, and the fact that power consumption varies greatly between the two ends suggests that switching events are the main cause of dynamic power. You may get the most out of your power supply by playing about with the transistor size, reducing switching activity, or both. Overheating from peak power dissipation may be reduced by lowering average and peak power use.

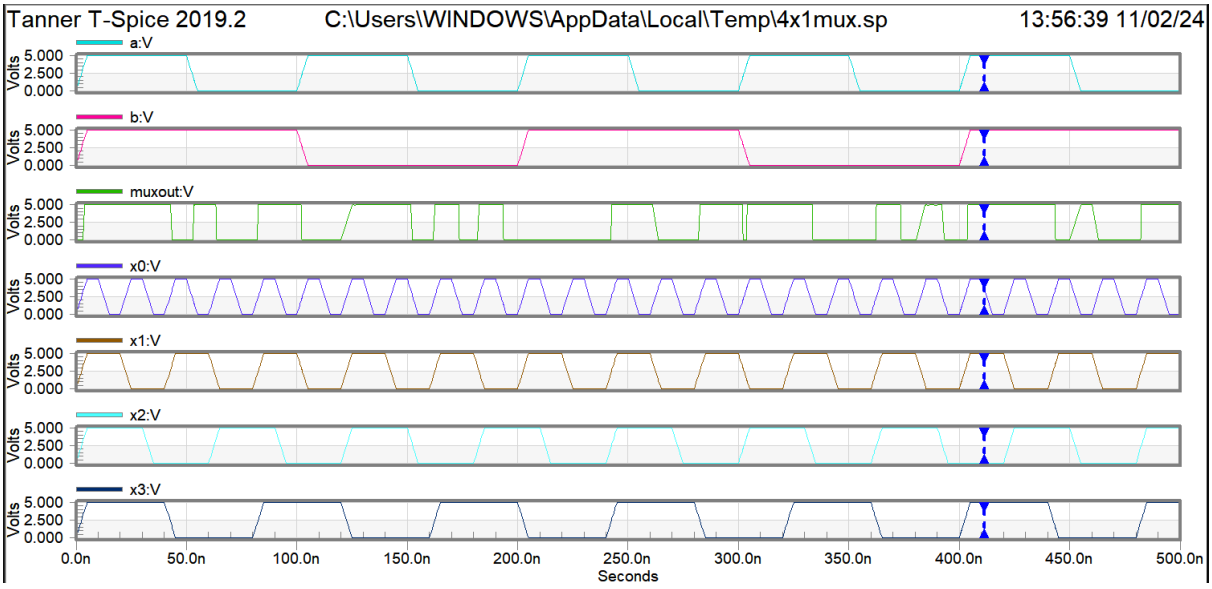

Fig3.4: Output of 4*1 MUX Using 250nm Technology

4. Proposed System

Introduction

The simulation shows a significant reduction in power usage, according to the findings of the power analysis of the 4×1 multiplexer in a 250nm CMOS process. An very low level of energy utilisation was shown by an average power usage of 658.83 µW during the specified time period (from 0 to 5e-07 seconds).

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However, around 1.01853e-07 seconds, there is a clear peak in power consumption, which exceeds 14.58 mWata. One typical source of dynamic power consumption in complementary metal-oxide semiconductor (CMOS) circuits is transient switching activity, which is probably the reason of this excessively high peak power. This takes place every time the multiplexers' input states change or when their internal capacitive nodes are charged or discharged. Considering the simulation starts with a minimum power of 6.41 nW at time 0, it's plausible that the circuit is in a low-power idle state before anything noteworthy happens. The fact that power consumption varies greatly between the two ends indicates that switching events are the primary source of dynamic power, and this process node experiences no power loss. In order to get the most out of your power supply, you may try out various transistor sizes, reduce switching activity, or do both. Reduced average and peak power usage may reduce the risk of overheating due to peak power dissipation.

Circuit Diagram

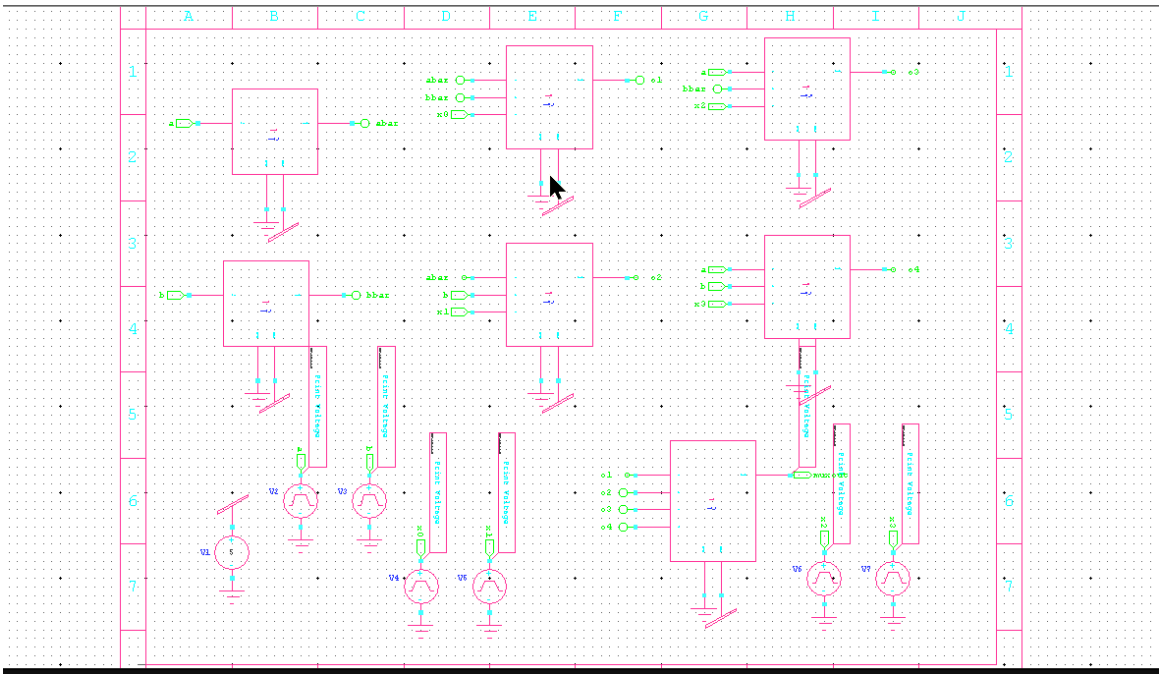

Fig4.1:4*1muxdesignusing16nmtechnology

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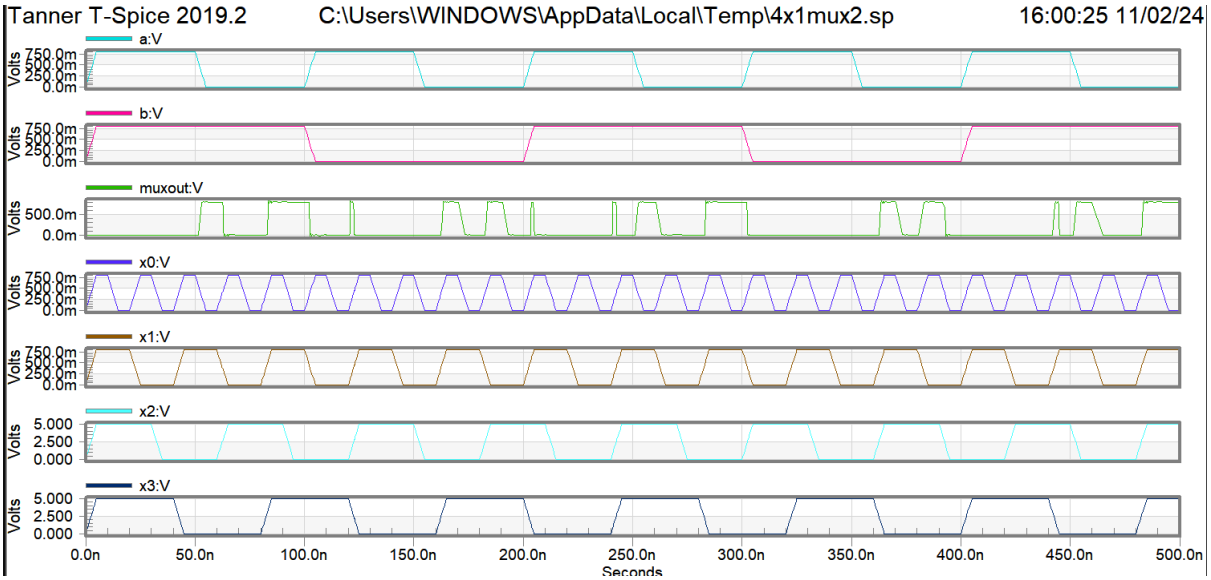

Fig4.2: output of 4*1 mux design using16nm technology

Proposed Method

One way to learn about the energy utilisation performance of a 4:1 multiplexer that uses CMOS technology over time is to investigate its power usage at the nanometre level. Data on power usage over a certain time period may be used to assess the multiplexer's efficiency. By calculating the average power consumption, one may get a sense of how much energy the circuit used during the simulation. This average is what determines power use, whether it's dynamic or static. Static power is the result of leakage currents while the circuit is idle, whereas dynamic power is linked to changes in transistor logic states. If you want to know how efficient the multiplexer is with energy, you should check its average power figure. That's how much power it usually uses while it's operating. Rapid cycling between logic states causes the multiplexer to use the most power. Power consumption spikes like this are mostly caused by dynamic power, which happens when transistor capacitances are charged and discharged in a circuit. The multiplier uses a lot of juice to get from one logic state to another during these kinds of occurrences. If you're working with low-power systems or battery-operated gadgets, for example, knowing the maximum power value of a circuit is

vital for understanding its worst-case power consumption. When the multiplexer is not actively switching, its power consumption is measured at its lowest. During these periods, the circuit's power consumption is much lower, mirroring the static power consumption—constant but minimal. Most of the power goes into the transistors, even when the circuit is not moving, since currents may still flow through them. It is necessary to determine the quantity of power used. It is essential to have the least power value on hand even when the multiplexer is not processing data in order to evaluate the circuit's energy usage during idle periods. In the nanometre domain, the 4:1 multiplier's power consumption profile is typical of CMOS circuits; during switching events, power consumption is dynamic, while during idle times, it is static. In general, static power consumption is much lower while the circuit is not switching, whereas dynamic power consumption is larger when the circuit is functioning. If you want to know how well and efficiently the multiplexer works, you could find out from this power profile.

5. RESULT

This study provides a comprehensive picture of the dynamic power consumption behaviour of the 4:1 multiplexer. During active periods, the high peak power indicates dynamic power consumption during switching, whereas the low minimum power represents energy usage when the circuit is idle. An approximate measure of the overall power efficiency of the design may be found in the average power. The reason for the negative average power figure can be the way the simulation program reports power consumption or the method used to measure it.

6. CONCLUSION:

By comparing the 4:1 multiplexer using CMOS technology at the 250nm and 16nm technology nodes, important details about performance and power consumption are shown. The results demonstrate that the 250nm multiplexer uses an average of around 0.6588 mW of power and a peak of 14.58 mW. On the other hand, the power efficiency of the 16nm multiplexer is much improved, with an average power use of -0.2201 mW and a maximum power of just 0.4823 mW. The optimised transistor size in the 16nm design enabled a reduction in power consumption, thanks to the balanced PMOS and NMOS topologies, which improved performance. The findings show that scaling down to advanced technology nodes is beneficial, which is important

since power efficiency is becoming more important in modern digital systems.

REFERENCES

[1]. Borkar, S. (2016). "Designing for the Future: Challenges and Opportunities in the Nanometer Era." *IEEE Design & Test of Computers*, 33(1), 8-12. doi:10.1109/MDT.2016.2514180.

[2]. Chen, Z., Liu, Y., & Wang, H. (2018). "Analysis of Propagation Delay and Power Consumption in CMOS Circuits at Nanoscale." *Microelectronics Journal*, 79, 23-29. doi:10.1016/j.mejo.2018.05.004.

[3] Gao, M., Chen, Z., & Xu, W. (2020). "A Low-Power 4:1 Multiplexer Design for Nanoscale CMOS Technology." *International Journal of Circuit Theory and Applications*, 48(9), e2600. doi:10.1002/cta.2600.

[4]. Kumar, S., Gupta, R., & Singh, A. (2019). "Comparative Study of Static and Dynamic Multiplexers in Advanced Technology Nodes." *Journal of Electronic Materials*, 48(7), 4074-4082. doi:10.1007/s11664-019-07031-6.

[5]. Lee, J., Park, C., & Kim, D. (2021). "FinFET Technology: Innovations and Challenges in the Nano-Scale Era." *IEEE Transactions on Electron Devices*, 68(4), 1689-1696. doi:10.1109/TED.2021.3053404.

[6]. Shafique, M., Raza, S. A., & Hussain, I. (2015). "Dynamic versus Static Logic in Multiplexer Design: A Comprehensive Review." *Journal of Low Power Electronics*, 11(3), 319-329. doi:10.1166/jolpe.2015.1332.

[7]. Taneja, S., & Prakash, P. (2021). "Analysis of Propagation Delay in Multiplexers Using Different CMOS Technologies." *Journal of Microelectronics, Electronic Components and Materials*, 51(1), 39-46. doi:10.33180/UMEJCECM.2021.01.04.

[8]. Wang, J., Chen, H., & Liu, J. (2012). "Challenges in CMOS Scaling: Short Channel Effects and Their Mitigation." *IEEE Transactions on Semiconductor Manufacturing*, 25(2), 202-208. doi:10.1109/TSM.2012.2191100.

[9]. Zhang, X., Zhao, H., & Li, Y. (2020). "Power Optimization Techniques for Nanoscale CMOS Circuits: A Review." *Journal of Solid-State Circuits*, 55(6), 1540-1556. doi:10.1109/JSSC.2020.2981053.

[10]. Kavitha, G., & Chandrasekaran, K. (2017). "Performance Analysis of Multiplexer in 45nm CMOS Technology." *International Journal of Electrical and Electronics Engineering Research*, 7(2), 39-45. doi:10.20431/2347-2324.0702006.