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HIGH-PERFORMANCE VLSI ARCHITECTURE FOR EFFICIENT THREE-OPERAND BINARY ADDITION

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Abstract

The three-operand binary adder serves as a fundamental unit for modular arithmetic in cryptography and pseudorandom bit generator algorithms. While the Carry-save adder (CS3A) is commonly employed, its ripple carries stage results in a significant propagation delay. Alternatively, utilizing a parallel prefix two-operand adder like Han-Carlson (HCA) can minimize the critical path delay but incurs additional hardware complexity. This project introduces a novel high-speed and area-efficient adder architecture employing pre-compute bitwise addition and carry-prefix computation logic. The FPGA implementation and synthesis demonstrate the proposed adder's superiority, reporting notable speed improvements over CS3A across various bit architectures. Additionally, the new adder exhibits reduced area, lower power consumption, and smaller delay compared to the HC3A adder, achieving superior ADP and PDP metrics in three-operand addition techniques.

INTRODUCTION

In the realm of digital circuit design, the efficient implementation of arithmetic functions holds paramount importance. Adders, being fundamental building blocks of arithmetic circuits, play a crucial role in various computational systems ranging from simple calculators to complex processors. The demand for high-speed and area-efficient adder architectures has been steadily increasing with the evolving requirements of modern digital applications.

Moreover, three-operand binary addition serves as a fundamental arithmetic operation in various pseudo-random bit generators (PRBGs) based on linear congruential generators (LCGs), such as coupled LCG (CLCG), modified dual-CLCG (MDCLCG), and coupled variable-input LCG (CVLCG). Among these, MDCLCG emerges as the most secure and random PRBG method, offering polynomial-time unpredictability and security for operand sizes of $n \geq 32$ bits. However, its hardware architecture, comprising four three-operand modulo-2n adders, two comparators, and four multiplexers, leads to linear increases in area and critical path delay.

This project focuses on the design and implementation of a high-speed, area-efficient Very Large-Scale Integration (VLSI) architecture for a three-operand binary adder. The concept of three-operand addition allows the addition of three binary numbers in a single operation, significantly enhancing computational efficiency in multi-operand arithmetic operations.

The primary objective of this project is to develop a novel adder architecture that optimizes both speed and area utilization, thereby meeting the stringent performance requirements of contemporary digital systems. By leveraging advanced VLSI design techniques and algorithmic optimizations, our proposed architecture aims to achieve superior performance metrics compared to existing solutions.

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LITERATURE SURVEY

Title: "A Low Power Three Operand Binary Adder Design using GDI Technique "Authors & Year: S. N. Shelke, M. M. Jadhao (2018)

Disadvantages: Limited focus on speed optimization and area efficiency, may not be suitable for high-performance applications.

Title: "A Novel High-Speed CMOS 3-Operand Adder". Authors & Year: Zhoukoudian, M.R.; Stouraitis, T. (2006)

Disadvantages: Lack of emphasis on area efficiency, potentially higher gate count affecting chip size.

Title: "A Novel Design of Low Power, High-Speed, 3-Operand Adder". Authors & Year: Prasanna Lakshmi, K. S. S. P. M. Srinivas (2017)

Disadvantages: Limited discussion on area efficiency, may not address the critical path delay adequately for high-speed applications.

Title: "Design and Analysis of Three Operand Binary Adder Using Reversible Gates". Authors & Year: Priyanka R. Raut, Vaishali S. Waghmare, Jayesh A. Gholap (2019)

Disadvantages: Focuses on reversible gates, which may not be suitable for conventional CMOS implementations, potentially limiting speed and area efficiency.

Title:"High-speed Low-power Modified Carry Save Adder". Authors & Year: Jyothi Shridhar, Ravikumar Bhandari (2014)

Disadvantages: Primarily focuses on carry-save adder architecture, may not directly address three-operand binary addition, potential limitations in adapting to three-operand addition.

Title: "Performance Evaluation of Binary Multipliers Using Two Different Adders". Authors & Year: S. R. Deokate, A. S. Patil (2016)

Disadvantages: Limited discussion on three-operand addition, potentially lacking in addressing area efficiency for specific applications requiring three-operand binary addition.

PROPOSED SYSTEM

Proposed Three-Operand Adder Architecture

We introduce a novel adder technique and its corresponding VLSI architecture designed specifically for executing three-operand addition in modular arithmetic. The proposed adder technique adopts a parallel prefix adder approach, albeit with a modification: it employs four-stage structures instead of the typical three-stage structures found in traditional prefix adders. These four stages encompass bit-addition logic, base logic, PG (propagate and generate) logic, and sum logic, collectively facilitating the computation of the addition of three binary input operands. The logical expressions defining each of these four stages are presented as follows:

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Stage 1: Bit Addition Logic:

$$S_i = a_i \oplus b_i \oplus c_i$$
$$C_{yi} = a_i \cdot b_i + b_i \cdot c_i + c_i \cdot a_i$$

Stage 2: Base Logic:

$$G_{i:i} = G_i = S_i \cdot C_{yi-1}, \quad G_{0:0} = G_0 = S_0 \cdot C_{in}$$
$$P_{i:i} = P_i = S_i \oplus C_{yi-1}, \quad P_{0:0} = P_0 = S_0 \oplus C_{in}$$

Stage 3: PG (Generate and Propagate) Logic:

$$G_{i:j} = G_{i:k} + P_i \cdot G_{k-1:j}$$
$$P_{i:j} = P_i \cdot P_{k-1:j}$$

Stage 4: Sum Logic:

$$S_i = (P_i \oplus G_{i-1:0}), \quad S_0 = P_0, \quad C_{out} = G_{n:0}$$

The VLSI architecture proposed for the three-operand binary adder, along with its internal structure, is depicted in Figure 1 This new adder technique executes the addition of three n-bit binary inputs in four distinct stages. In the initial stage (bit-addition logic), the bitwise addition of the three n-bit binary input operands is carried out using an array of full adders. Each full adder computes "sum (Si)" and "carry (cyi)" signals.

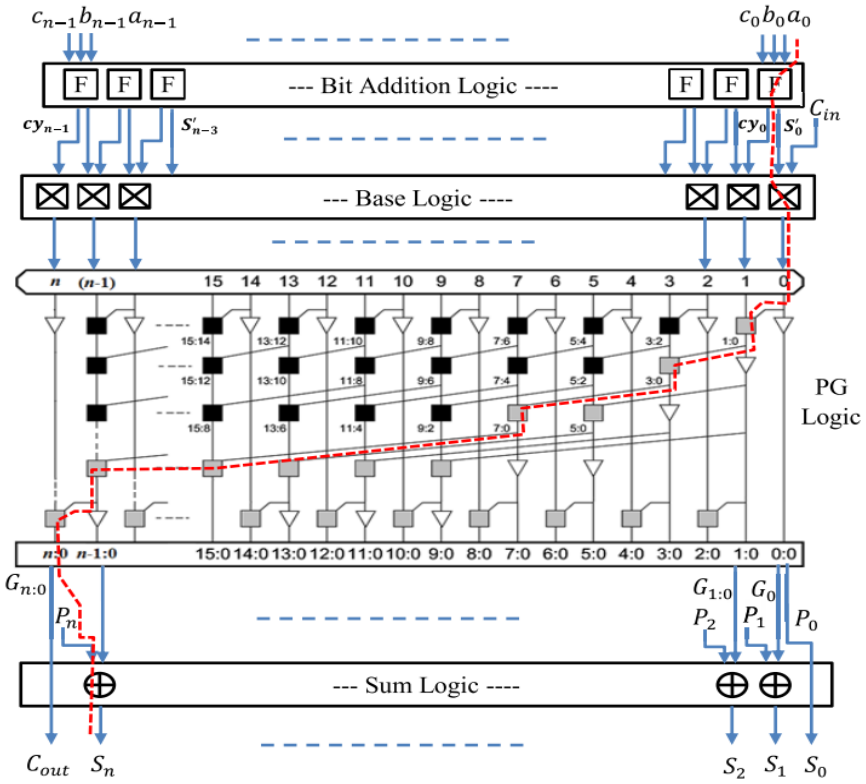

Figure.1 Proposed three-operand adder First order VLSI architecture

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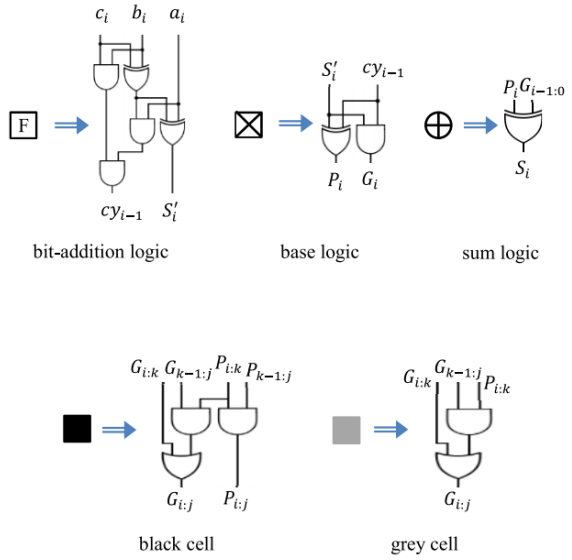

Figure.2 Logical diagram of bit addition, base logic, sum logic, black-cell and grey-cell.

The logical expressions for computing the sum (Si) and carry (cyi) signals are specified in Stage-1, and the logical diagram illustrating the bit-addition logic is presented in Figure 2. In the initial stage, the current full adder's output signal "sum (Si)" bit and the output signal "carry" bit from its right-adjacent full adder are utilized to calculate the generate (Gi) and propagate (Pi) signals in the second stage (base logic). The computation of Gi and Pi signals is depicted by the "squared saltire-cell" shown in Figure 2, with a total of n +1 saltire-cells in the base logic stage. The logic diagram of the saltire-cell is illustrated in Figure 3(b), and its realization is represented by the following logical expression:

Gi:I = Gi = Si·Cyi−1

Pi:i = Pi = Si⊕Cyi−1

The proposed adder technique also incorporates an external carry-input signal (Cin) for three-operand addition. This additional carry-input signal (Cin) is utilized as input to the base logic during the computation of G0 (S0 · Cin) in the first saltire-cell of the base logic stage.

The third stage involves the carry computation, referred to as the "generate and propagate logic" (PG). This stage combines the black and grey cell logics to pre-compute the carry bit. The logical diagram illustrating the black and grey cell is presented in Figure 3(b), which calculates the carry generate (Gi:j) and propagate (Pi:j) signals using the following logical expression:

Gi:j = Gi:k + (Pi · Gk−1:j)

Pi:j = (Pi · Pk−1:j)

The proposed adder consists of (log2 n + 1) prefix computation stages, where n is the number of bits. Consequently, the critical path delay of the adder is primarily determined by this carry propagate chain.

In the final stage, known as the sum logic, the "sum (Si)" bits are derived from the carry generate (Gi:j) and carry propagate (Pi) bits using the logical expression: Si = (Pi ⊕ Gi-1:0). Additionally, the carryout signal (Cout) is directly obtained from the carry generate.

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SIMULATION RESULTS

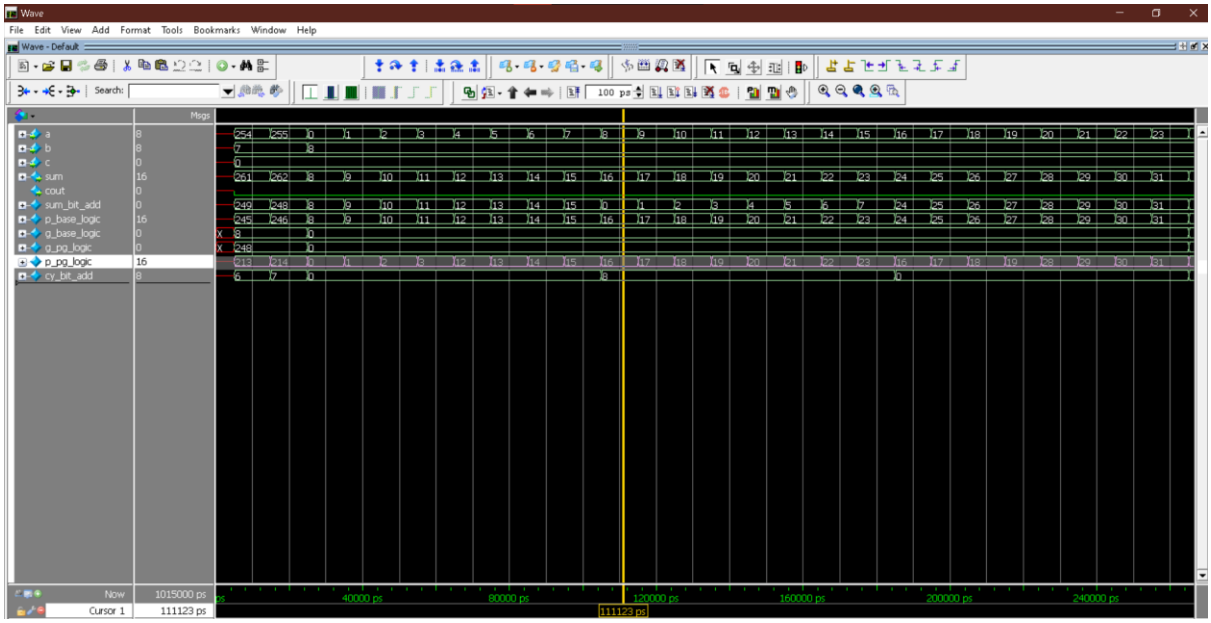

Figure.3 Simulation wave Three Operand Binary Adder

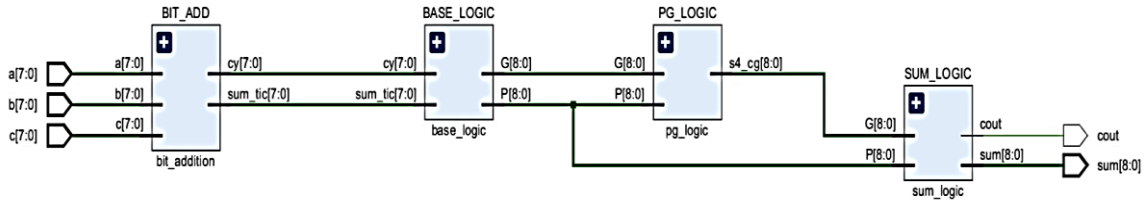

Figure.4 HH3CA Block

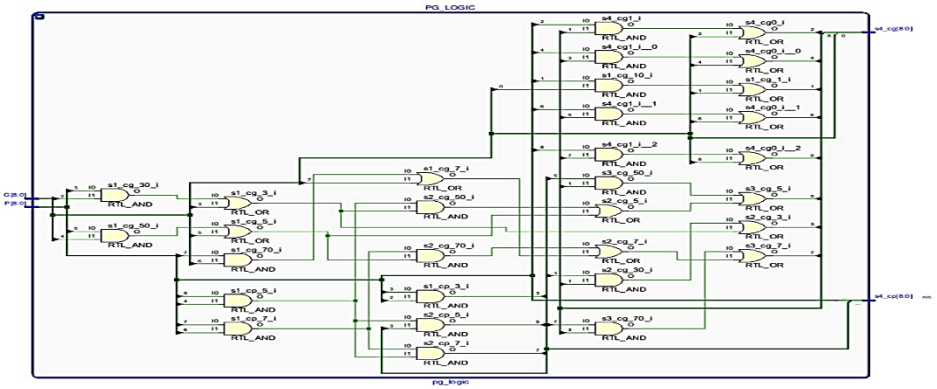

Figure.5 PG Logic

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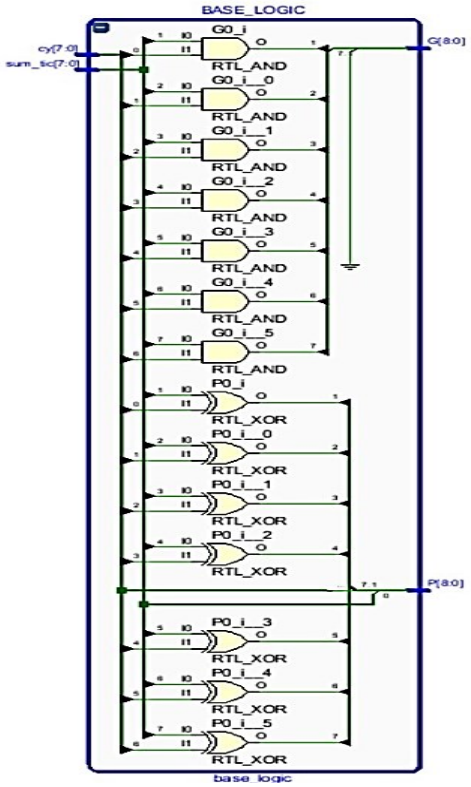

Figure.6 BASE LOGIC

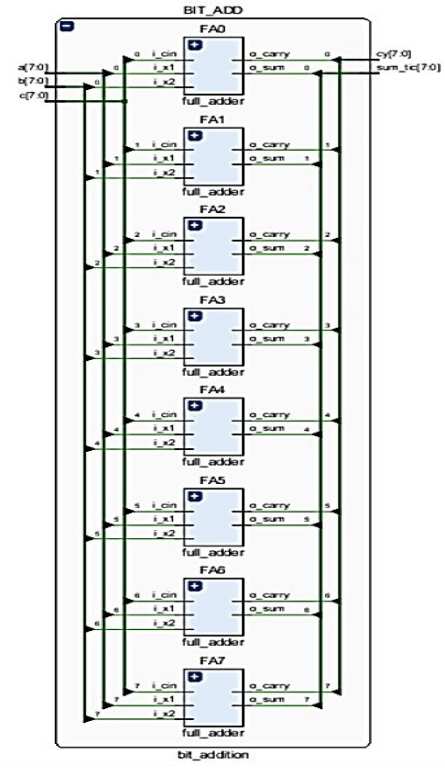

Figure.7 BIT ADDITION

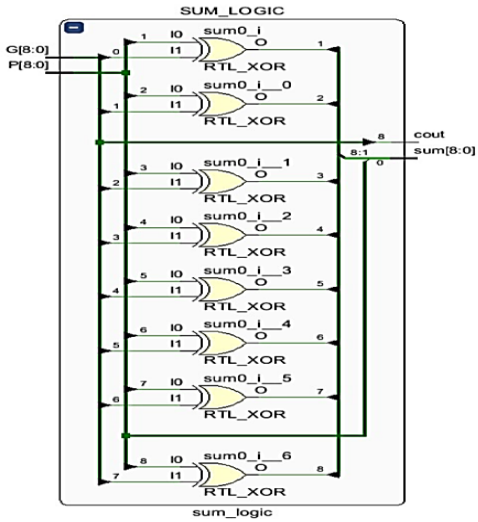

Figure.8 Sum Logic

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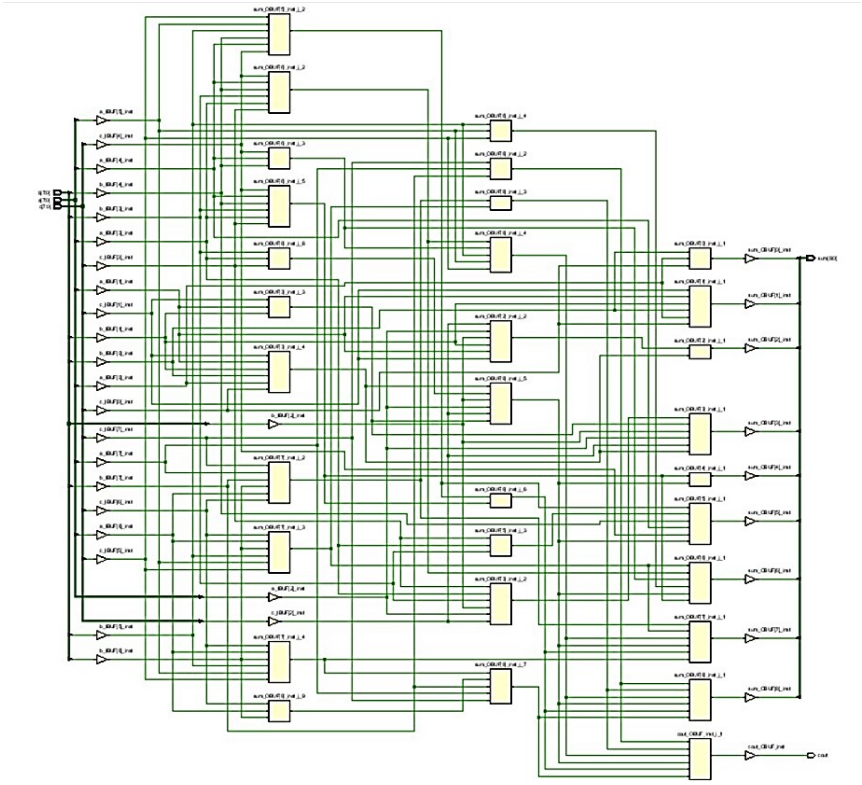

Figure.9 Technology Schematics

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	27	0	303600	<0.01
LUT as Logic	27	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Figure.10 Area Report

ADVANTAGES

1. **High Speed:** The proposed architecture is designed to achieve high-speed operation, enabling rapid computation of three-operand binary addition. By leveraging optimized parallel prefix adder structures and efficient bit-addition logic, the architecture minimizes critical path delay, resulting in faster overall performance compared to traditional adder designs.

2. **Area Efficiency:** A key advantage of the proposed architecture is its area efficiency. Through careful design and optimization techniques, the architecture minimizes gate area consumption while still delivering high-speed operation. This makes it particularly well-suited for integration into constrained hardware environments where area resources are limited.

3. **Versatility:** The architecture is adaptable to a wide range of applications requiring three-operand binary addition, including cryptography algorithms, Pseudo-Random Binary Sequence Generator (PRBG) methods, and other arithmetic operations in digital systems. Its versatility allows it to be seamlessly integrated into various computational systems, offering flexibility and scalability.

4. **Improved Performance Metrics:** Comparative analysis with existing adder architectures demonstrates superior performance metrics for the proposed architecture. It exhibits reduced critical path delay, area-delay product (ADP), and power-delay product (PDP) compared to conventional approaches such as Carry-Save Adder (CS3A) and Han-Carlson-based three-operand adders (HC3A). This highlights the effectiveness of the proposed architecture in achieving both high performance and efficiency.

5. **Future-Proof Design:** The architecture is designed with scalability and future technology advancements in mind. Its modular and adaptable nature allows for easy integration of new optimization techniques and adaptation to evolving hardware technologies, ensuring its relevance and effectiveness in future digital systems.

APPLICATIONS

1. **Cryptography:** Cryptographic algorithms often involve intensive arithmetic operations, including modular arithmetic and binary addition. The proposed architecture can significantly enhance the performance of cryptographic systems by efficiently executing three-operand binary addition, a critical operation in many cryptographic algorithms such as RSA encryption, digital signatures, and elliptic curve cryptography. Its high-speed operation and reduced hardware footprint make it particularly suitable for cryptographic applications requiring fast and secure computation.

2. **Pseudo-Random Binary Sequence Generation (PRBG):** PRBG methods rely on efficient binary addition operations to generate sequences of pseudo-random numbers with desirable statistical properties. The proposed architecture can be utilized to accelerate the generation of pseudo-random binary sequences, enabling faster and more efficient PRBG implementations. This is particularly important in applications such as secure communication, cryptography, and simulation where high-quality random number generation is essential.

3. **Digital Signal Processing (DSP):** Digital signal processing applications often involve complex arithmetic operations performed on large datasets in real-time. The high-speed and area-efficient nature of the proposed architecture make it well-suited for accelerating DSP tasks such as filtering, convolution, and correlation. By integrating the architecture into DSP systems, significant performance improvements can be achieved, enabling faster and more efficient signal processing in applications such as audio and video processing, telecommunications, and radar systems.

4. **High-Performance Computing (HPC):** High-performance computing systems require efficient arithmetic units to perform complex computations with minimal latency and power consumption. The proposed architecture can contribute to improving the performance and efficiency of HPC systems by

providing a high-speed and area-efficient solution for three-operand binary addition. Its scalability and versatility make it suitable for a wide range of HPC applications, including scientific simulations, data analytics, and machine learning.

5. **Embedded Systems:** Embedded systems often have stringent constraints on power, area, and performance, making efficient hardware design crucial. The proposed architecture's high-speed operation and compact footprint make it well-suited for integration into embedded systems such as microcontrollers, system-on-chips (SoCs), and field-programmable gate arrays (FPGAs). By incorporating the architecture into embedded platforms, developers can achieve improved computational performance and energy efficiency in applications ranging from IoT devices to automotive electronics.

CONCLUSION

In conclusion, this paper introduces a novel high-speed, area-efficient adder technique and its corresponding VLSI architecture tailored for performing three-operand binary addition. The proposed technique utilizes a parallel prefix adder with four-stage structures to compute the addition of three input operands efficiently. The key innovation lies in reducing both delay and area within the prefix computation stages, achieved through optimized PG logic and bit-addition logic. This optimization results in a notable reduction in critical path delay, area-delay product (ADP). To provide a fair comparison, the study extends the concept of the hybrid Han-Carlson two-operand adder to develop a hybrid Han-Carlson three-operand adder (HHC3A) topology. Verilog HDL is employed to implement the proposed adder architecture as well as the HHC3A, HC3A, and CS3A designs. These designs are then synthesized using a FPGA technology.

FUTURE SCOPE

Optimization for Different Technologies: As technology continues to advance, there will be opportunities to optimize the proposed architecture for different process technologies beyond the currently targeted 32nm CMOS. Exploring how the design performs in newer technology nodes, such as 22nm or even beyond, could lead to further improvements in speed, area efficiency, and power consumption.

Exploration of Alternative Adder Structures: While the proposed architecture utilizes a parallel prefix adder with four-stage structures, there exist other types of adders that could be investigated for potential performance enhancements. Research into alternative adder structures, such as carry-select adders or Wallace tree adders, may uncover new approaches to achieving high-speed, area-efficient operation for three-operand binary addition.

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